ECN	REV	DESCRIPTION
DCN 105	01	See notes 1
DCN 108	02	See notes 2
DCN 119	03	See notes 3
	04	See Note 4

Notes:

1. Initial Release. Circuit design equivalent to CWRU PM1B with changed manufacture of several resistors and capacitors for manufacture and supplie r conformity.

2. - Added Part Number MURATA - GCM21BR72A104KA37K to C1 and C6
   - Added Part Number MURATA GRM188R61H105KAALD to C2, 14, 15, 30, 38, 40, 41, 42.
   - Added Part Number Vishay Siliconix - SI1026X-T1-E3 to U17
   - Added Part Number Texas Instruments - SN74LVC2G02YEAR to U20 and U21
   - Added Part Number Linear Technology -LT1964ES5-BYP#TRMPBF to U9
   - Added Part Number NDK NX5032GA-8.000Mto Y1

3. - Changed U24 from Texas Instuments REF3312AIDCKR (SC70-3) to REF3312AIDBZR (SOT23-3) to match the PCB footprint.
   - Removed Date and Approved blocks from the history block of the schemnatic template

4. - Changed C33 from a 330pF to 330nF (0.33uF)

51-2002-01 Pulse Generator (PG4)

	BY	DATE
DRAWN	R. Yoder	2/19/2020
CHECKED	A. Zbrzeski	2/19/2020

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DOCUMENT NAME: Schematic table of contents. Revision History.

SIZE	DOCUMENT NUMBER	REV.
B	51-2002-01	04

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NAME **PG4**

Pulse Generator with 4 channels

SYMBOLS

Symbols are optional and for clarification purposes only.

ANALOG SIGNALS

- reversing polarity variable amplitude analog signal
- fixed polarity variable amplitude analog signal
- fixed polarity constant amplitude analog signal
- current regulated passive recovery stimulus pulse
- biopotential signal
- radiofrequency link
- near field link

DIGITAL SIGNALS

- high level true
- low level true
- pulse width modulated

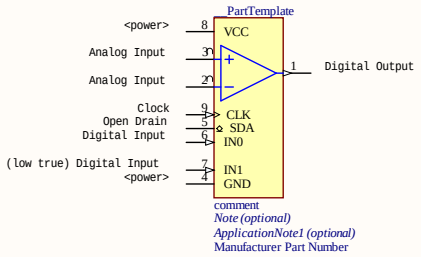
MIXED SIGNALS

- FESCAN bus power and data signal

ANALOG CURRENT FLOW or DIGITAL SIGNAL DIRECTION

- bidirectional
- unidirectional
- unidirectional

COMPONENT LABELLING



PAGE LIST

MODULE SYSTEMS GROUPING

-x,-1x non-tissue interfaces
-2x power conditioning
-3x RESERVED for internal energy systems
-4x processing
-6x tissue interfaces

MODULE SYSTEMS LIST

-1 MODULE HEADER SYSTEM
-2 TEST HEADER SYSTEM
-11 NETWORK DATA INTERFACE SYSTEM

-21 NETWORK POWER INTERFACE SYSTEM
-22 3V3 POWER SUPPLY SYSTEM
-23 VOS POWER SUPPLY SYSTEM

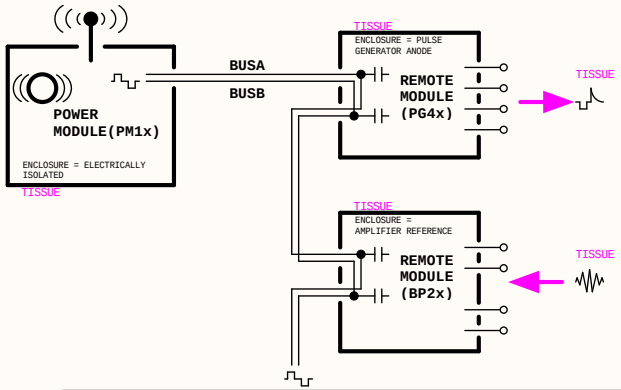
-41 MICROCONTROLLER SYSTEM
-42 DIGITAL PERIPHERAL SYSTEM
-43 ANALOG PERIPHERAL SYSTEM

-61 PULSE GENERATION SYSTEM

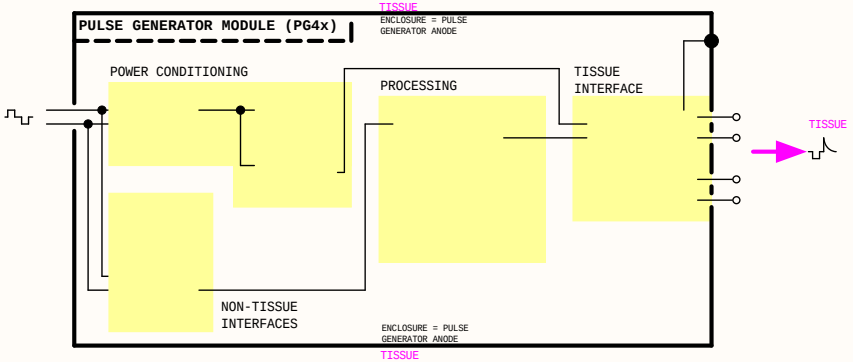
DESIGN NOTES

1) 3V3 and GND are global power objects and not shown for clarity
2) All resistors 1% unless otherwise specified.
3) Rx = Resistor,Inductor,Diode
4) Kx = Integrated Circuit
5) Xx = Connector
6) Power supply resistor guidance: R1=series input, R2=series output
7) Qx = Switch
8) DRH = Design Rating for Hardware
9) DRS = Design Rating for Software

TYPICAL APPLICATION



BLOCK DIAGRAM



DESIGN RATINGS FOR HARDWARE

	_Group	_Min	_Nom	_Max	_Units	_Desc
DRH1	VIN			10	V	Max from LT3464
DRH2	3V3	3.15	3.3		V	Min from MAX5355
DRH3	ADC0			2.56	V	Max if using internal AREF
DRH4	ADC1			2.56	V	Max if using internal AREF
DRH5	ADC2			2.56	V	Max if using internal AREF
DRH6	ADC3			2.56	V	Max if using internal AREF
DRH7	VOS			34	V	Max from LT3464

DESIGN RATINGS FOR SOFTWARE

	_Group	_Desc
DRS1	PUD	MCUCR register's Pull Up Disable (PUD) bit must remain at default (zero)
DRS2	TXCAN	TXCAN (PD5) must be forced HIGH-LOW-HIGH or LOW-HIGH-LOW on every power cycle
DRS3	ADC0	ADC0 (PF0) must be set as an analog input
DRS4	ADC1	ADC1 (PF1) must be set as an analog input
DRS5	ADC2	ADC2 (PF2) must be set as an analog input
DRS6	ADC3	ADC3 (PF3) must be set as an analog input
DRS7	ADC4	ADC4 (PF4) must be set as an analog input when not in programming mode
DRS8	ADC5	ADC5 (PF5) must be set as an analog input when not in programming mode
DRS9	HEARTBEAT	PG2 should be set low in final software to reduce power consumption.

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DOCUMENT NAME	Documentation 1	
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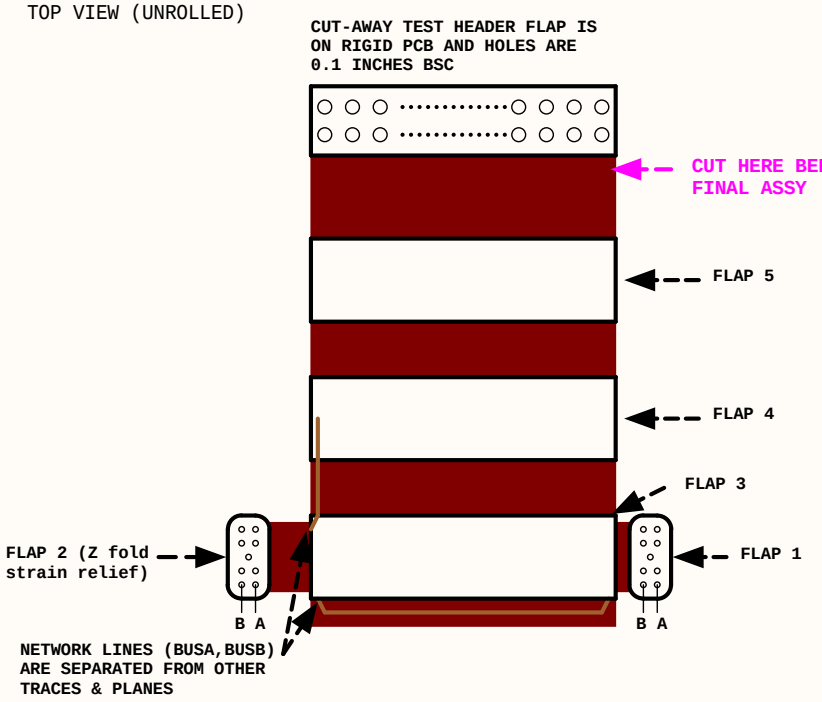
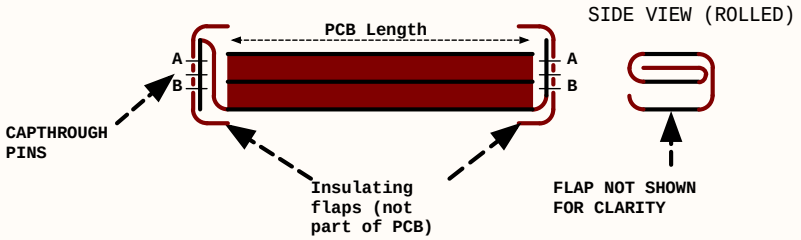
MECHANICAL LEGEND

- through hole
- top & bottom test pad with via
- PCB trace
- Enclosure connection pin
- flex PCB only
- rigid-flex PCB

TOP VIEW (UNROLLED)

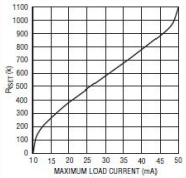


SIDE VIEW (ROLLED)



SIDE VIEW (ROLLED)

LTC3642 DC BUCK LOAD CURRENT LIMIT VS. RSET

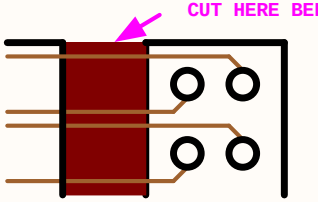


PROCESSOR FUSE SETTINGS

FUSE NAME	SETTING	RATIONALE
BODLEVEL	2.7V	Most appropriate setting when running off of a 3.3V rail.
TAOSEL	*DISABLE*	*Reserved for factory test.*
OCDEN	*DISABLE*	*On-Chip Debugger disabled to save power. Can be used in development.*
JTAGEN	ENABLE	Enable JTAG programming.
SPIEN	ENABLE	Enable SPI programming.
WDTON	*DISABLE*	*Watchdog timer disabled to prevent reset when in bootloader.*
EESAVE	*DISABLE*	*Do no preserve EE memory through chip erase.*
BOOTSZ	4096,$F000	CAN bootloader needs as much space as possible.
BOOTRST	ENABLE	Forces module to enter bootloader after reset.
CKDIV8	*DISABLE*	*Clock is divided in bootloader/application code only.*
CKOUT	*DISABLE*	*Do not push clock out to PC7 (CLK0).*
SUT_CKSEL	[1],[2]	[1] Ext. Crystal Osc. 8.0- MHz [2] Start-up time: 16K CK + 0mS

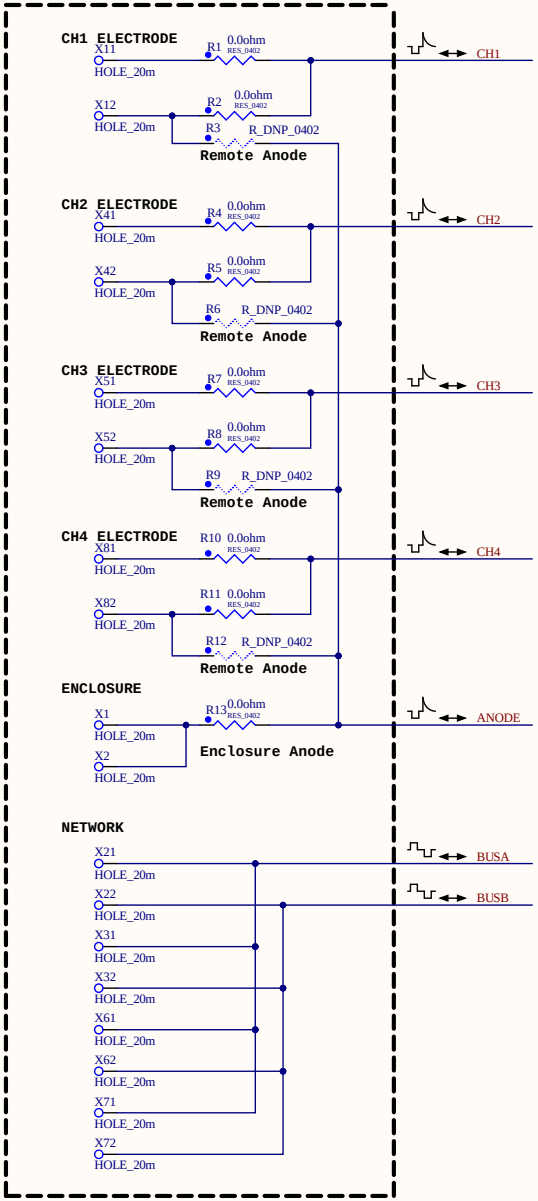
External crystal oscillator is used to ensure high accuracy CAN clock. Need to minimize start-up time when module used on a pulse powered network.
(NOTE: 16K CK @ 8 MHz = 2ms)

LR1 Do not place adjacent-layer copper traces to the cut-away header

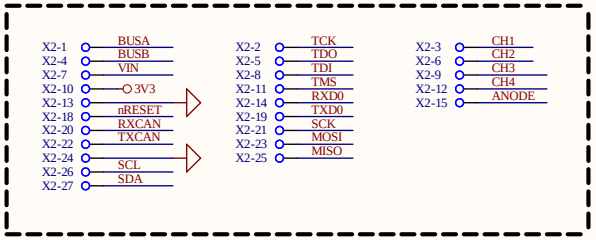


DOCUMENT NAME	Documentation 2	
SIZE B	DOCUMENT NUMBER 51-2002-01	REV. 04
	SHEET 3 OF 8	

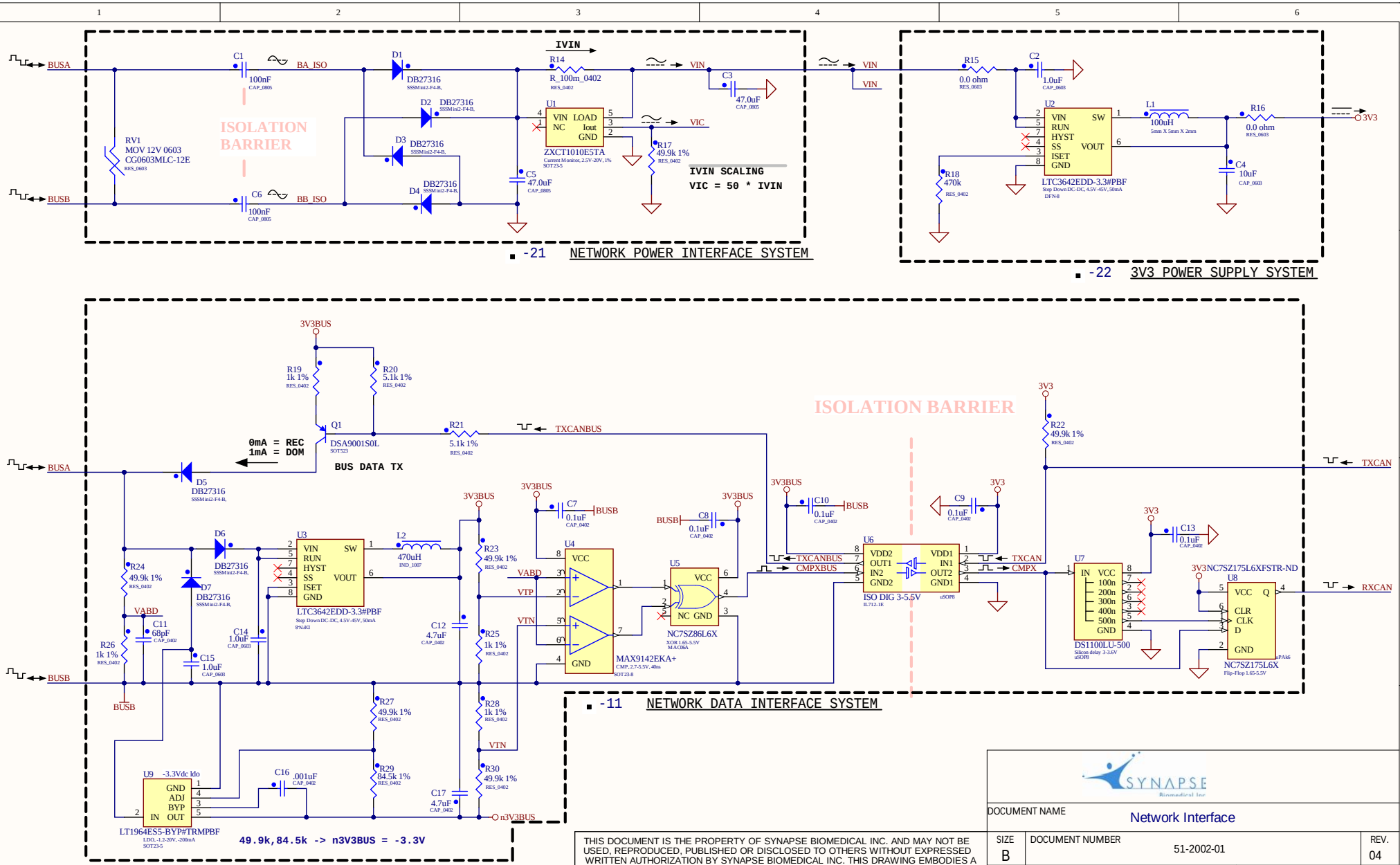
-1 MODULE HEADER SYSTEM



-2 TEST HEADER SYSTEM



DOCUMENT NAME	Modular and test header	
SIZE B	DOCUMENT NUMBER 51-2002-01	REV. 04
	SHEET 4 OF 8	



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DOCUMENT NAME: Network Interface

SIZE: B | DOCUMENT NUMBER: 51-2002-01 | REV.: 04

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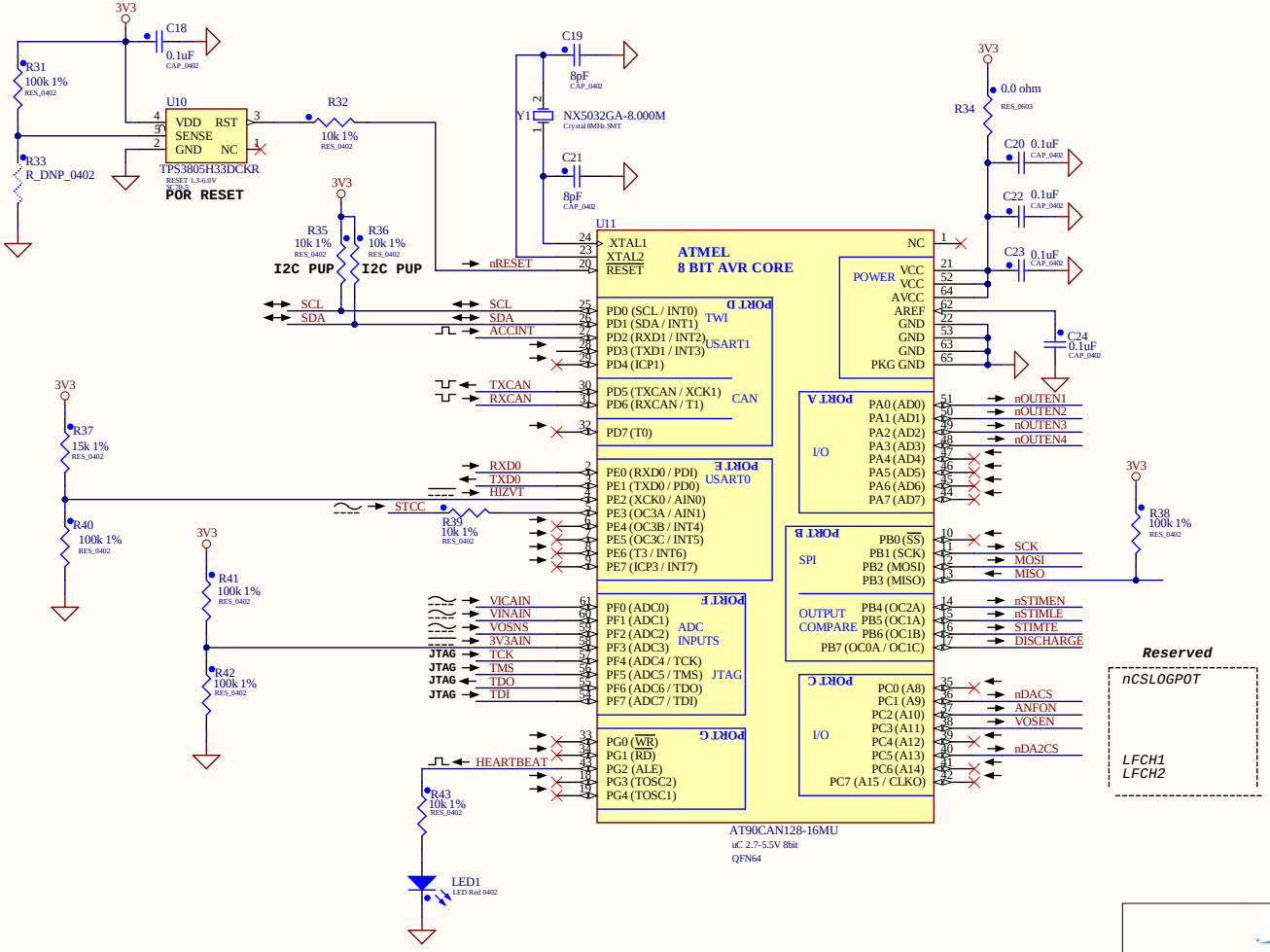
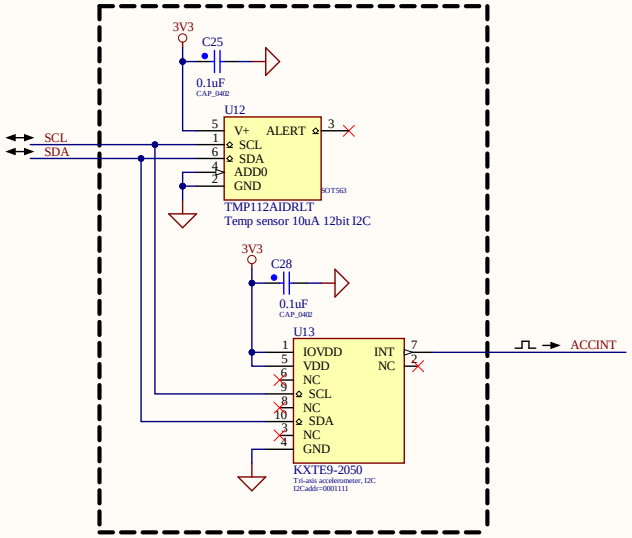
-41 MICROCONTROLLER SYSTEM

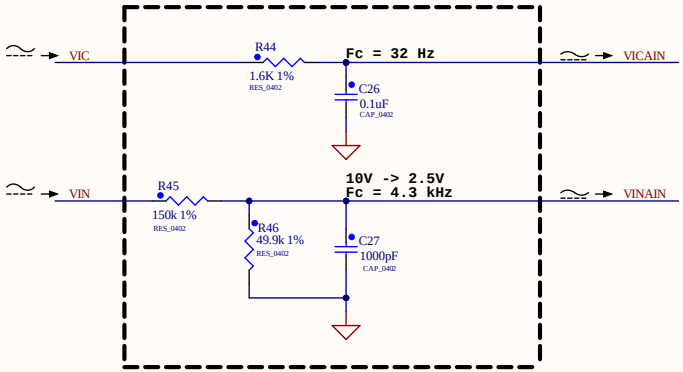


DOCUMENT NAME	PG4 Microcontroller
SIZE: B	DOCUMENT NUMBER: 51-2002-01
REV.: 04	
SHEET 6 OF 8	

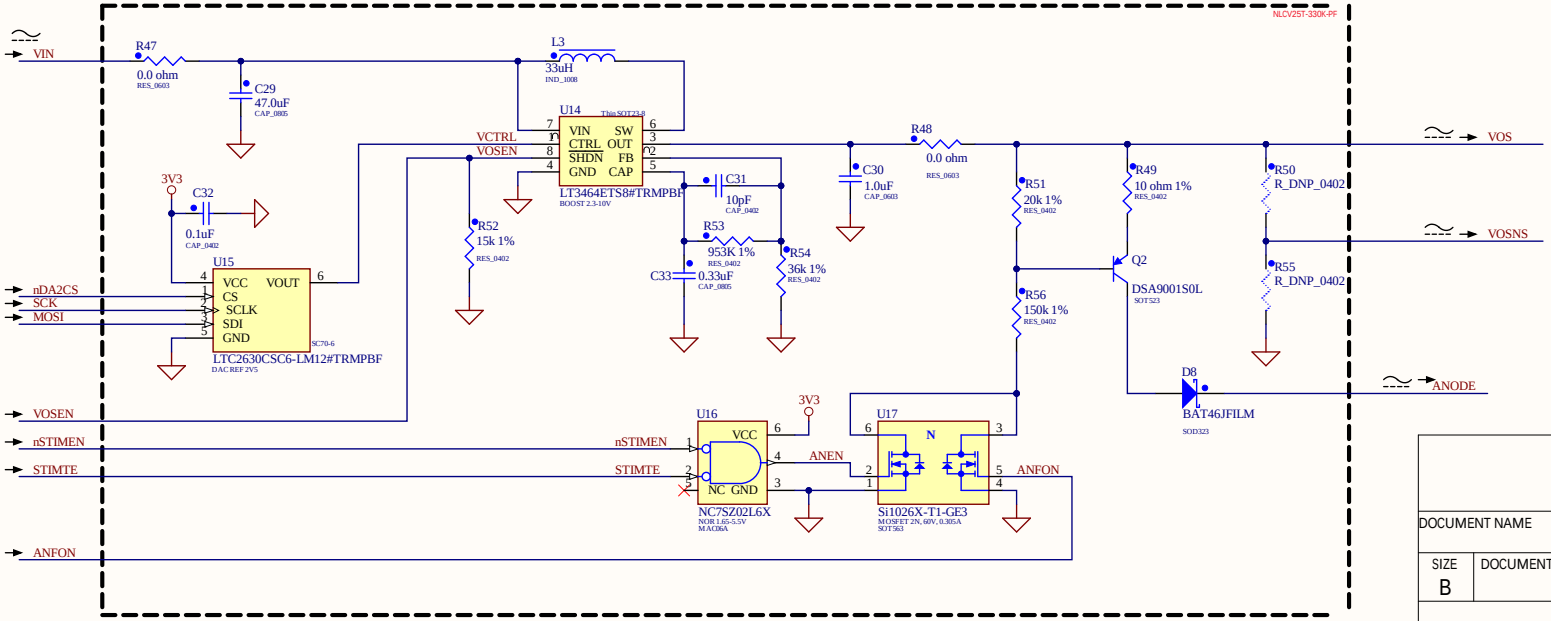
-42 DIGITAL PERIPHERAL SYSTEM



-43 ANALOG PERIPHERAL SYSTEM



-23 VOS POWER SUPPLY SYSTEM



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DOCUMENT NAME	VOS Power Supply System Analog/Digital Peripheral System	
SIZE B	DOCUMENT NUMBER 51-2002-01	REV. 04
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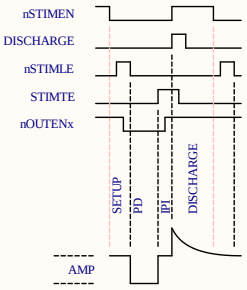
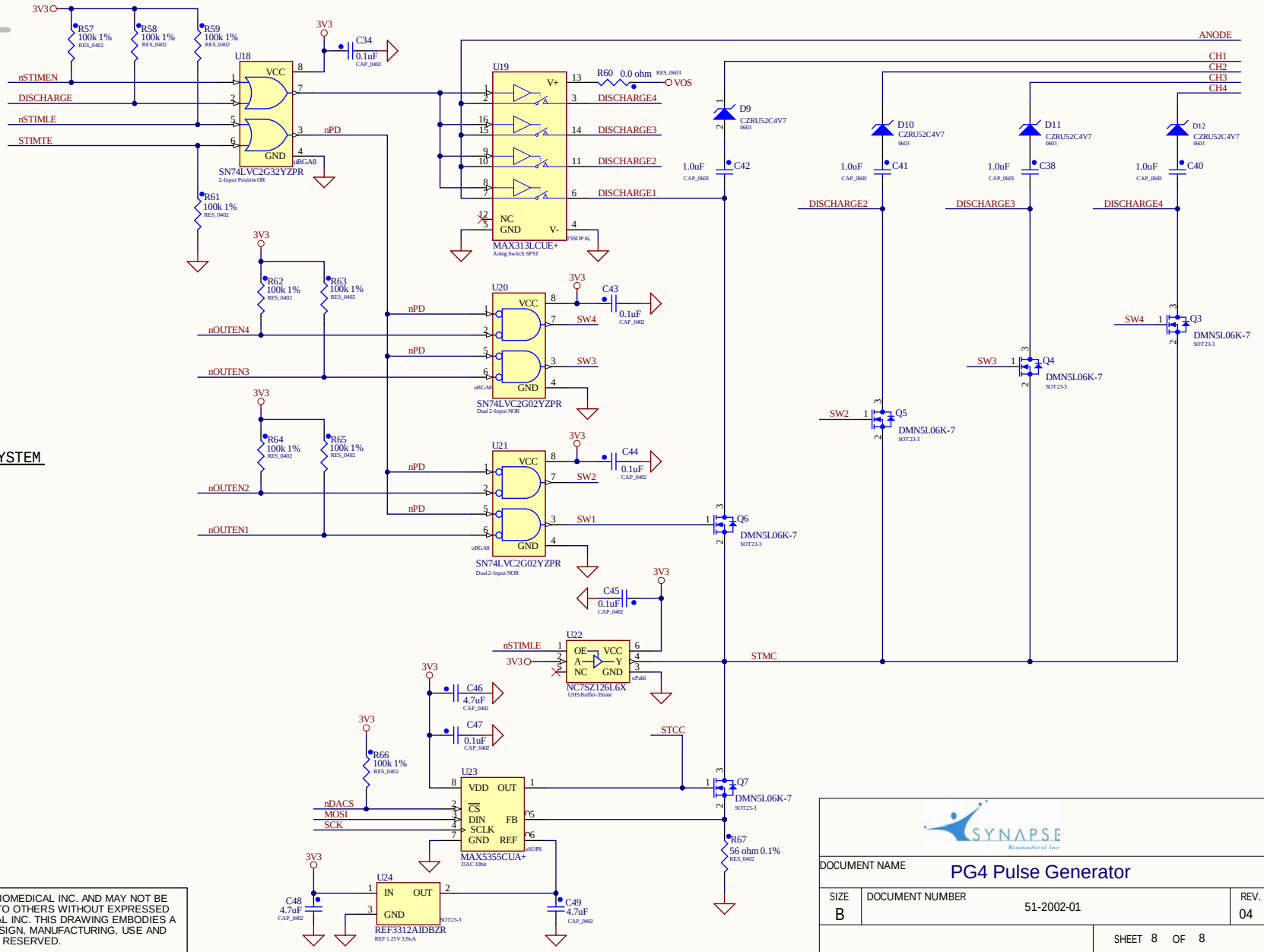
PULSE GENERATION SEQUENCE



Interval	Description
SETUP	SETUP current AMPlitude
PD,AMP	regulate current AMPlitude for Pulse Duration
IPI	wait for InterPhase Interval
DISCHARGE	DISCHARGE charge balancing capacitors

- -61 PULSE GENERATION SYSTEM



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DOCUMENT NAME: PG4 Pulse Generator

SIZE	DOCUMENT NUMBER	REV.
B	51-2002-01	04

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