Table of Contents & Revision History

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Signal Nomenclature

File: PM1C_Rev_1_Signal_Definition.kicad_sch

Block Diagram & FESCAN Timing

File: PM1C_Rev_1_FESCAN_Timing.kicad_sch

Test Interface

File: PM1C_Rev_1_Test_Interface.kicad_sch

MED Radio

SCK1
MOSI1
MISO1

Microcontroller

SCK1
MOSI1
MISO1
LOAD_AN
VNET_AN
VREC_AN
VSYS_AN
TXD0
RXD0
SCK0
MISO0
MOSI0
nTRST_LPC
TMS_LPC
TCK_LPC
RTCK_LPC
TDI_LPC
TDO_LPC
CPLD10
TXCAN
RXCAN
I2CS0
I2CS1
DISCHG
nSHDNBT1
nSHDNCHG1
nSHDNBT2
nSHDNCHG2
nSHDNBT3
nSHDNCHG3
CCBT
SCLOCK
SDATA
THRM
nCSFLA
nCSRAM
ACCINT

Near-Field Link

VSYS
SCLOCK
SDATA
VREC

Power Supply

VSYS
LOAD_AN
VSUPPLY

Network Power

VSUPPLY
VNET
SCLOCK
SDATA

Analog Voltage Monitoring

VNET
VNET_AN
VSYS
VREC_AN
VREC
VSYS_AN

Test Points

SCK1
MOSI1
MISO1
TXD0
RXD0
SCLOCK
SDATA
SCK0
MISO0
MOSI0
nTRST_LPC
TMS_LPC
TCK_LPC
RTCK_LPC
TDI_LPC
TDO_LPC
RXCAN
TXCAN

CPLD

CPLD10
TXCAN
RXCAN
I2CS0
I2CS1
DISCHG
DISCHG1
DISCHG2
DISCHG3
nSENSE
nSNSEN
nPHA
nOEB
nPHB
SNSEN
SCKSEL1
SCKSEL2
SCKSEL3

Network Drive & Network Current Sense

nSENSE
nSNSEN
nPHA
nOEB
nPHB
SNSEN

Module Connector

Battery 1 Conditioning

VSYS
nSHDNBT1
nSHDNCHG1
CCBT
DISCHG1
SCLOCK1
SDATA1

Battery 2 Conditioning

VSYS
nSHDNBT2
nSHDNCHG2
CCBT
DISCHG2
SCLOCK2
SDATA2

Battery 3 Conditioning

VSYS
nSHDNBT3
nSHDNCHG3
CCBT
DISCHG3
SCLOCK3
SDATA3

I2C Multiplexing

SCLOCK1
SDATA1
SCLOCK2
SDATA2
SCLOCK3
SDATA3
SCLOCK
SDATA
SCKSEL1
SCKSEL2
SCKSEL3

Thermister & Digital Peripheral System

SCLOCK
SDATA
THRM
nCSFLA
nCSRAM
ACCINT
SCK0
MOSI0
MISO0

Sheet: /
File: PM1C_Rev_1_2.kicad_sch

Title:

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KiCad E.D.A. 8.0.2		Id: 1/20

Power Module (PM)

Note 1, KiCAD translation of Altium Power Module Design

Initial KiCAD version of PM1C Rev 0 is equivalent to Altium version of PM1B Rev 4

Note 2, Rev 1

Update to match Module Connector

Schematic table of contents.

Sheet: /Table of Contents & Revision History/
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Title:

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KiCad E.D.A. 8.0.2		Id: 1/20

ANALOG SIGNALS

- reversing polarity variable amplitude analog signal
- fixed polarity variable amplitude analog signal
- fixed polarity constant amplitude analog signal
- current regulated passive recovery stimulus pulse
- biopotential signal
- radiofrequency link
- near field link

DIGITAL SIGNALS

- high level true
- low level true
- pulse width modulated

MIXED SIGNALS

FESCAN bus power and data signal

ANALOG CURRENT FLOW or DIGITAL SIGNAL DIRECTION

- bidirectional
- unidirectional
- unidirectional

COMPONENT LABELLING

PART TEMPLATE

<power>	VCC
Analog Input	
Clock	CLK
Open Drain Output	SDA
Digital Input (high true)	IN0
Digital Input (low true)	\IN1
<power>	GND

comment
Note (optional)
Application Note (optional)
Manufacturer Part Number

MODULE SYSTEMS

MODULE SYSTEM GROUPING

-x,-1x non-tissue interfaces
-2x power conditioning
-3x internal energy systems
-4x processing
-6x tissue interfaces

MODULE SYSTEMS LIST

-1 MODULE HEADER SYSTEM
-2 ENCLOSURE THERMISTOR SYSTEM
-3 TEST HEADER SYSTEM
-11 CPLD SYSTEM
-12 NETWORK DRIVE SYSTEM
-13 NETWORK CURRENT SENSE SYSTEM
-14 RADIO SYSTEM

-21 NEAR FIELD LINK SYSTEM
-22 4V6 POWER SUPPLY SYSTEM
-23 MODULE CURRENT SENSE SYSTEM
-24 3V3 POWER SUPPLY SYSTEM
-25 N3V3 POWER SUPPLY SYSTEM
-26 1V8 POWER SUPPLY SYSTEM
-27 NETWORK POWER SUPPLY SYSTEM

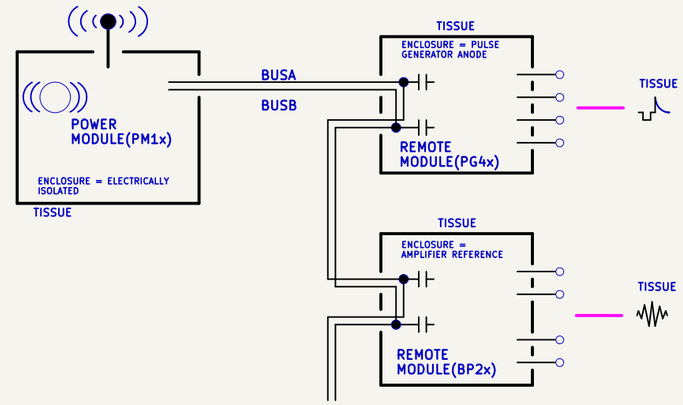
BATTERY CONDITIONING SYSTEMS
-31 BATTERY 1 CONDITIONING SYSTEM
-32 BATTERY 2 CONDITIONING SYSTEM
-33 BATTERY 3 CONDITIONING SYSTEM

-41 UCONTROLLER SYSTEM
-42 DIGITAL PERIPHERAL SYSTEM
-43 ANALOG PERIPHERAL SYSTEM
-44 I2C MULTIPLEXING SYSTEM

DESIGN NOTES

1) 3V3 and GND are global power objects and not shown for clarity
2) Unless otherwise specified, all resistors have 1% tolerance

TYPICAL APPLICATION



DESIGN RATINGS

	MIN	NOM	MAX	UNITS	DESCRIPTION
VSYS	2.6	4.6	5.5	V	MIN from LTC4411, Max from LM3670MF-1.8 and LTC3440
VBR	6.3	20	34	V	MIN & MAX from LT1933
VREC	6.3	20	34	V	MIN & MAX from LT1933
VNET	4.5		10	V	MIN from EL7156, MAX from LT3464
P0.7		3.3		V	P0.7 Set High to enable SPI master.
P0.20		3.3		V	P0.20 Set High to enable SPI master.
P1.20		3.3		V	P1.20 Set High tp disable TRACE port.
P1.26		0		V	P1.26 has internal Pull-up.

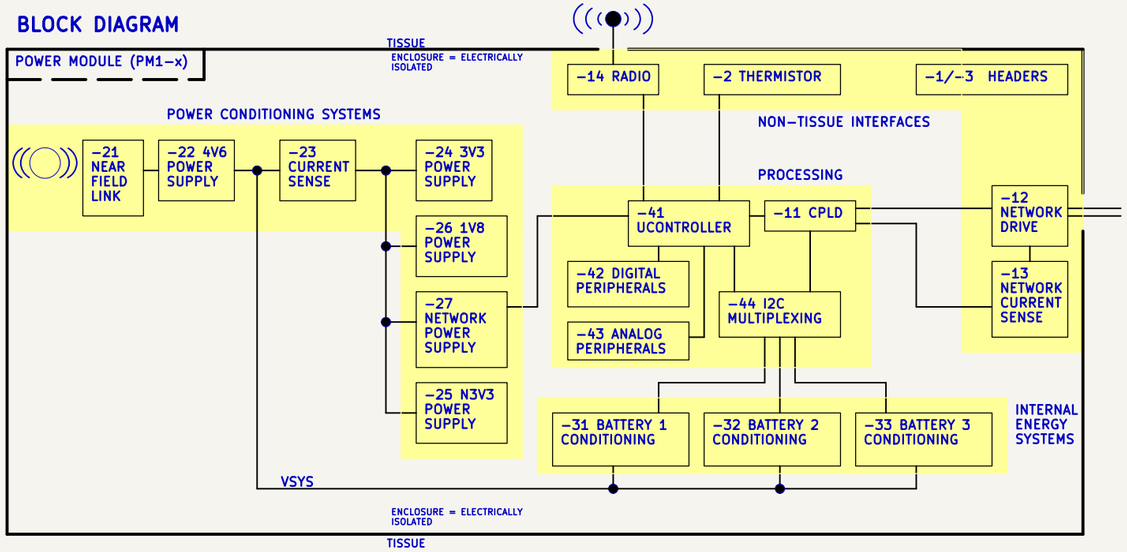
_DRT1	VSYS	2.6	4.6	5.5	V	Min from LTC4411,Max from LM3670MF-1.8 and LTC3440
_DRT2	VBR	6.3	20	34	V	Min,Max from LT1933
_DRT3	VREC	6.3	20	34	V	Min,Max from LT1933
_DRT4	VNET	4.5		10	V	Min from EL7156,Max from LT3464 on PG4
_DRT11	P0.7		3.3		V	P0.7 set high to enable SPI master.
_DRT12	P0.20		3.3		V	P0.20 set high to enable SPI master.
_DRT13	P1.20		3.3		V	P1.20 set high to disable TRACE port.
_DRT14	P1.26		0		V	P1.26 has interanl PUP.

Sheet: /Signal Nomenclature/
File: PM1C_Rev_1_Signal_Definition.kicad_sch

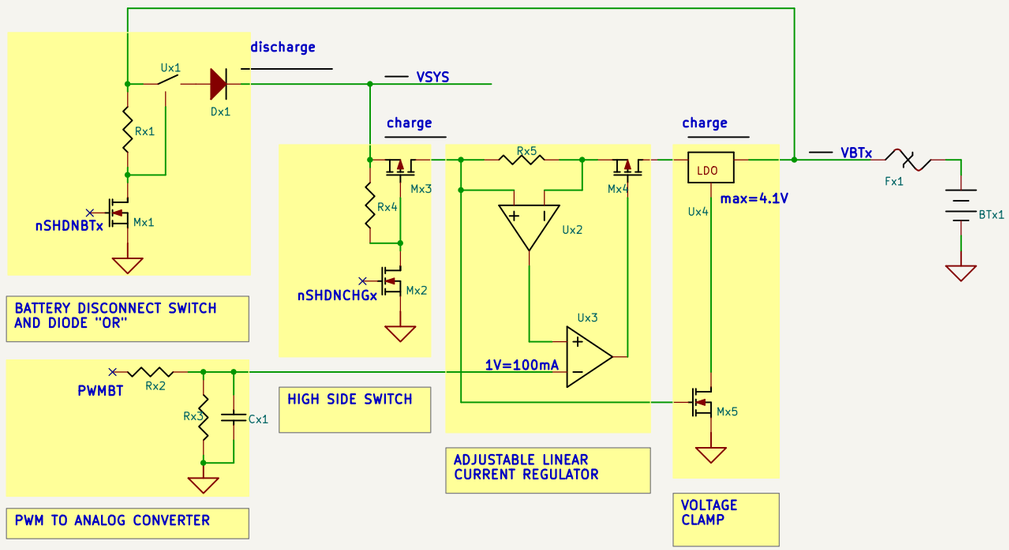
Title:

Size: B	Date:	**Rev: –**
KiCad E.D.A. 8.0.2		Id: 1/20

BLOCK DIAGRAM



BLOCK DIAGRAM FOR A SINGLE BATTERY CONDITIONING SYSTEM

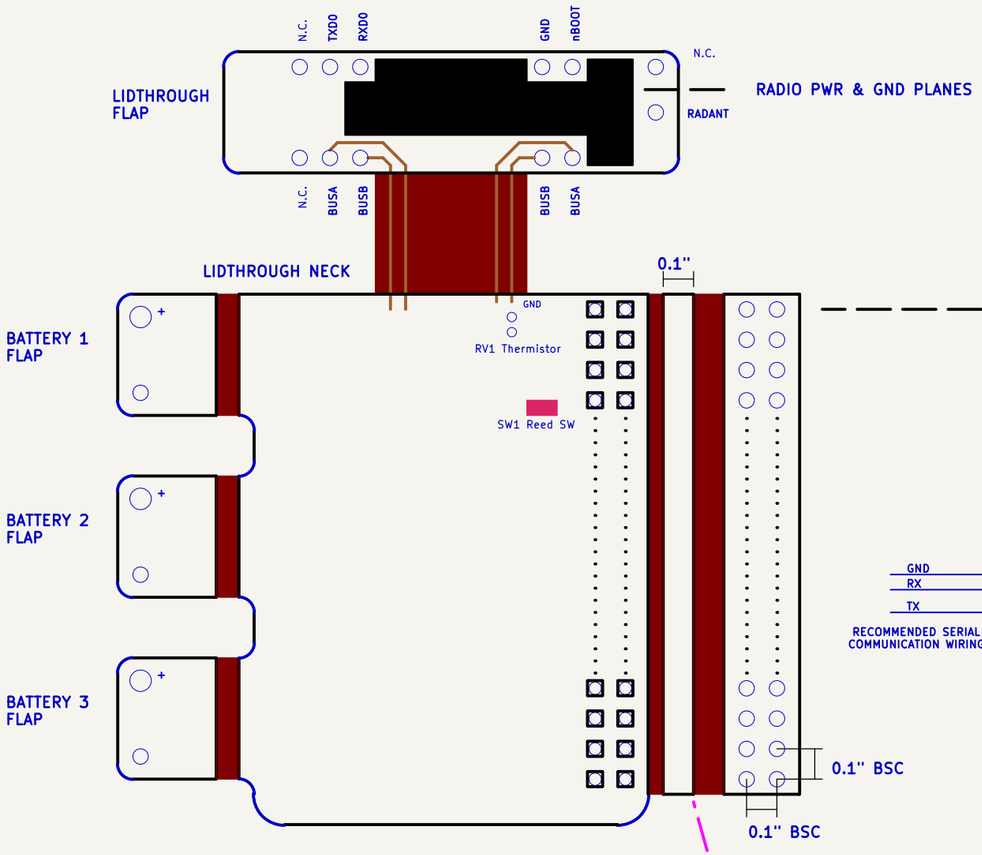


Sheet: /Block Diagram & FESCAN Timing/
File: PM1C_Rev_1_FESCAN_Timing.kicad_sch

Title:

Size: B	Date:	Rev: –
KiCad E.D.A. 8.0.2		Id: 1/20

TOP SIDE FEATURES



MECHANICAL LEGEND

- through hole
- top & bottom test pad with via
- PCB trace
- flex PCB only
- rigid–flex PCB

TEST HEADER PINOUT

36	RTCK_LPC	GND	35
34	TDI_LPC	VREC	33
32	TDO_LPC	1V8	31
30	TMS_LPC	n3V3	29
28	TCK_LPC	VNET	27
26	nTRST_LPC	VSUPPLY	25
24	nBOOT	VSYS	23
22	nDRESET	SDATA	21
20	nRESET	SCLOCK	19
18	GND	GND	17
16	RXD0	MISO1	15
14	TXD0	MOSI1	13
12	TMS_CPLD	SCK1	11
10	TDI_CPLD	MISO0	9
8	TDO_CPLD	MOSI0	7
6	TCK_CPLD	SCK0	5
4	GND	TXCAN	3
2	3V3	RXCAN	1

RECOMMENDED BOOTLOADER ENTRY METHOD

RECOMMENDED RESET METHOD

GND
RX
TX
RECOMMENDED SERIAL COMMUNICATION WIRING

NEAR FIELD COIL SIMULATION CONNECTION

CAUTION: VREC VOLTAGE WILL DESTROY CIRCUIT IF APPLIED TO OTHER PINS

VREC
20 VDC (100mA limit)

RECOMMENDED TEST POWER CONNECTION

VSYS
3.7 VDC (200mA limit)

Frame Mounting Holes

M3 M4 M5 M6

ASSEMBLY NOTES

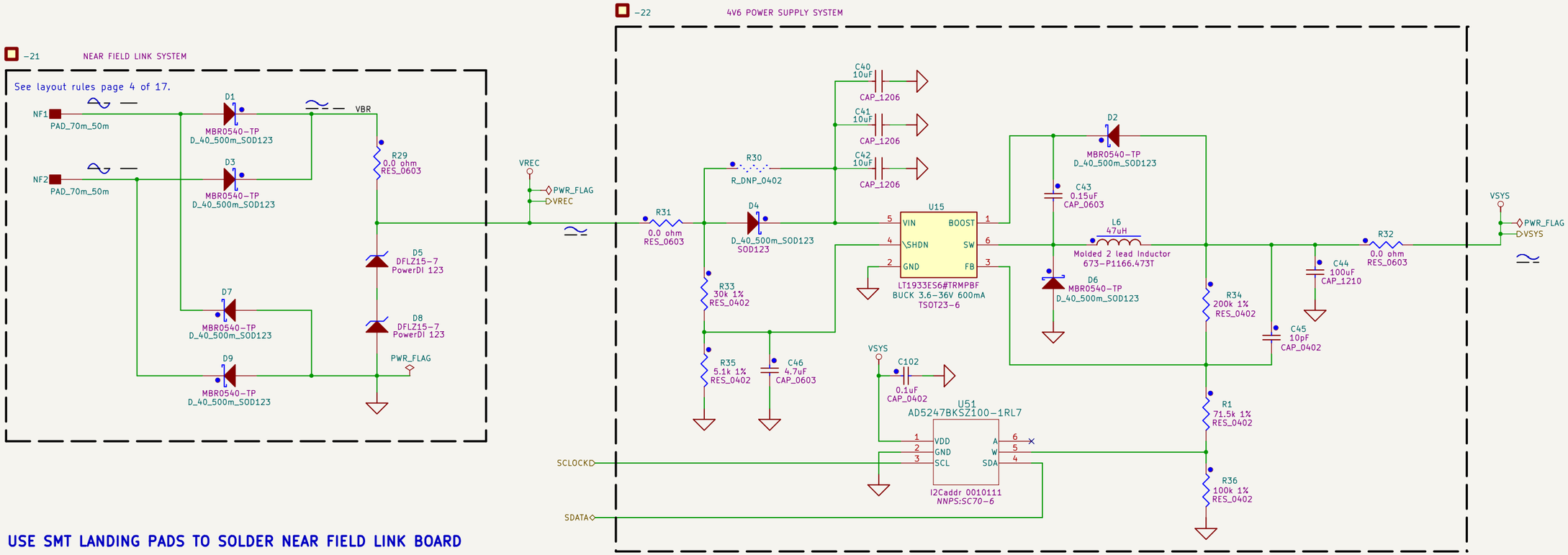
CUT FLEX AS CLOSE AS POSSIBLE TO THIS FLAP BEFORE FINAL ASSY

FLAP IS ADHERED TO COIL DURING FINAL ASSY FOR MECHANICAL STABILITY

Sheet: /Test Interface/
File: PM1C_Rev_1_Test_Interface.kicad_sch

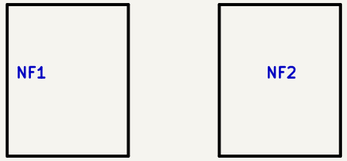
Title:

Size: B | Date: | **Rev: –**
KiCad E.D.A. 8.0.2 | Id: 1/20

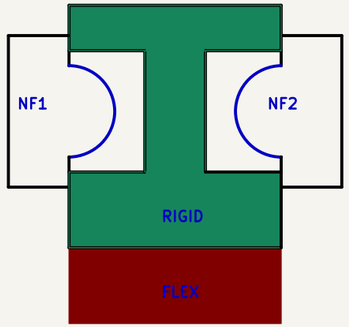


USE SMT LANDING PADS TO SOLDER NEAR FIELD LINK BOARD

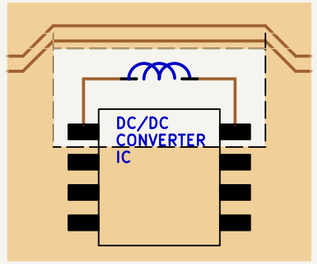
PM1x LANDING PADS ONLY



PM1x SOLDERED TO NF1x



LAYOUT RULES



CUTOUT PLANES AND DO NOT ROUTE UNDERNEATH HIGH CURRENT SWITCHING LOOPS

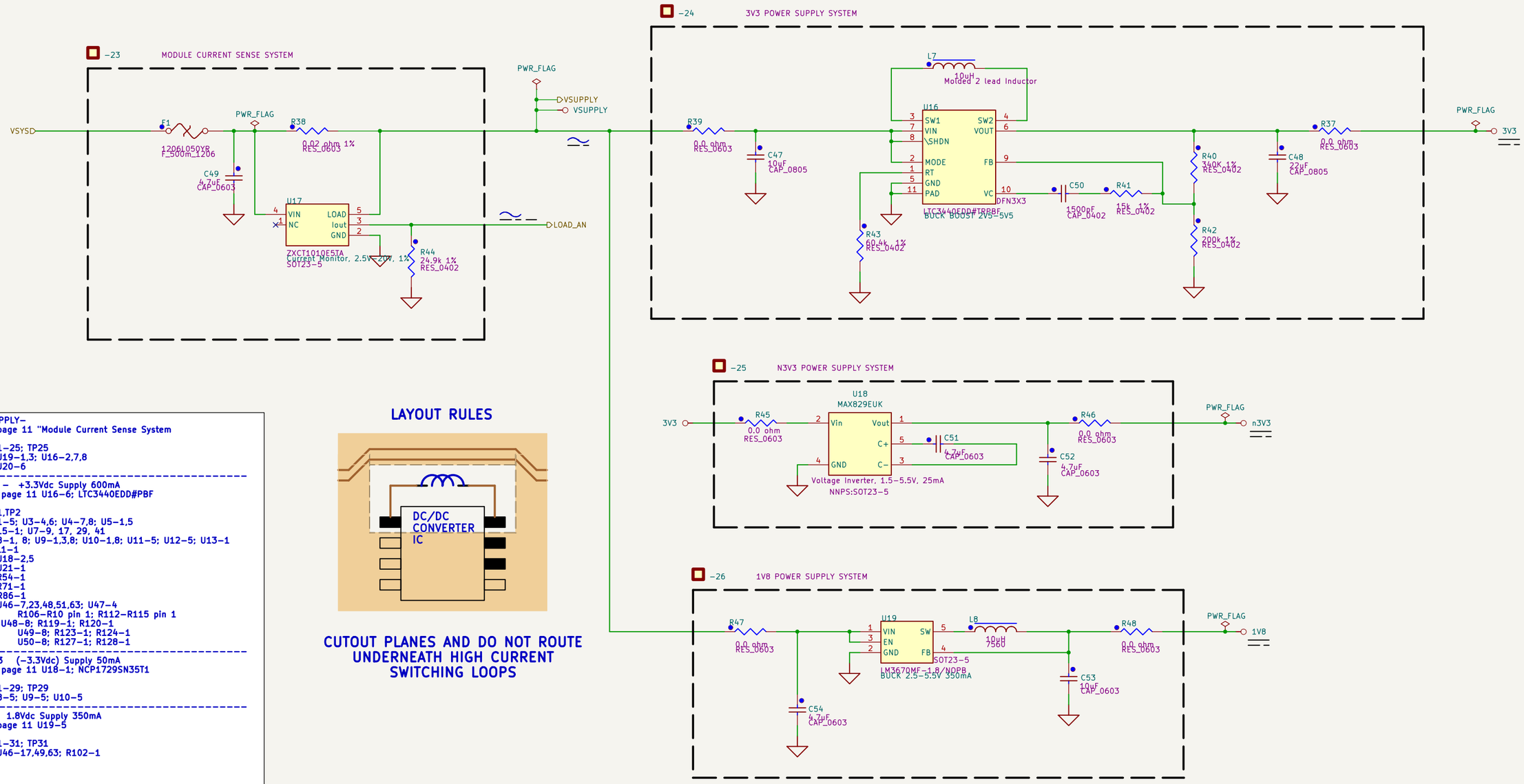
DESIGN RATINGS

	MIN	NOM	MAX	UNITS	DESCRIPTION
VSYS	2.6	4.6	5.5	V	MIN from LTC4411, Max from LM3670MF-1.8 and LTC3440
VBR	6.3	20	34	V	MIN & MAX from LT1933
VREC	6.3	20	34	V	MIN & MAX from LT1933
VNET	4.5		10	V	MIN from EL7156, MAX from LT3464
P0.7		3.3		V	P0.7 Set High to enable SPI master.
P0.20		3.3		V	P0.20 Set High to enable SPI master.
P1.20		3.3		V	P1.20 Set High tp disable TRACE port.
P1.26		0		V	P1.26 has internal Pull-up.

Sheet: /Near-Field Link/
File: PM1C_Rev_1_Near_Field.kicad_sch

Title:

Size: B | Date: | **Rev: -**
KiCad E.D.A. 8.0.2 | Id: 1/20



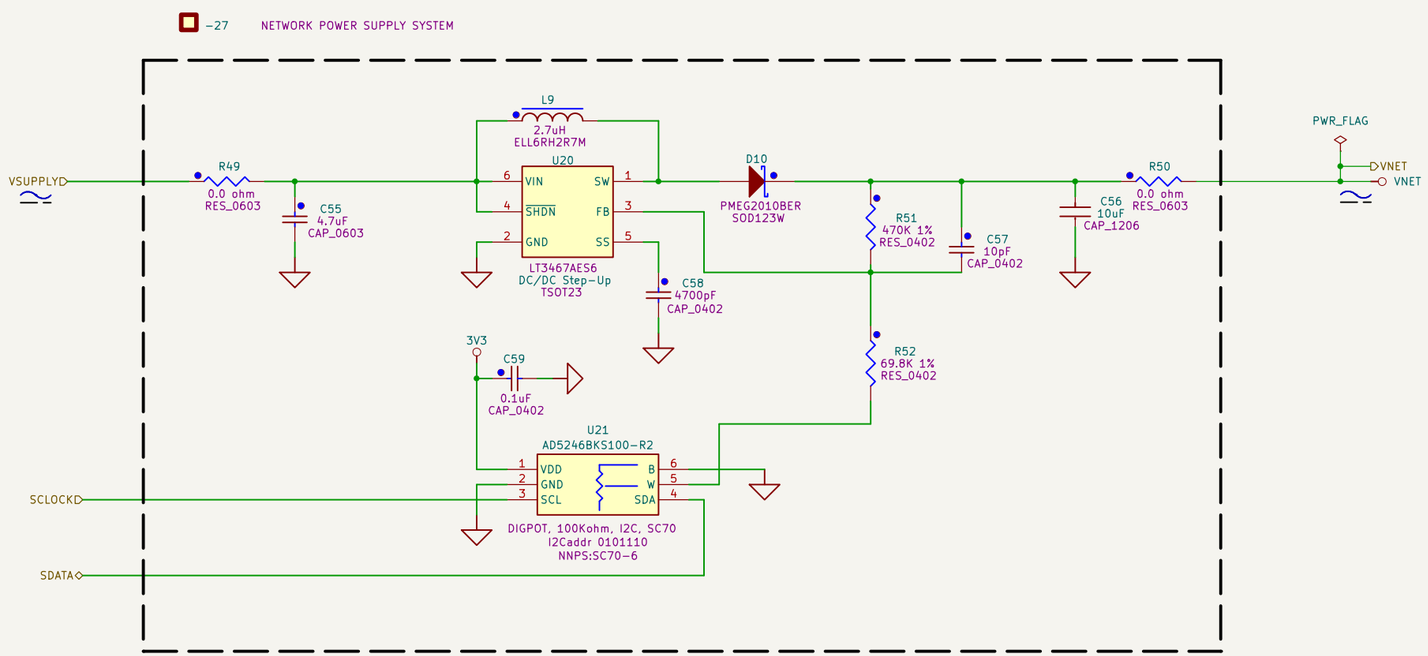

```
Net- VSUPPLY-
Source- page 11 "Module Current Sense System
Circuit
page 6 H1-25; TP25
page 12 U19-1,3; U16-2,7,8
page 13 U20-6
-----------------------------------------
Net- 3V3 -  +3.3Vdc Supply 600mA
Source - page 11 U16-6; LTC3440EDD#PBF
Circuit
page 6 H1,TP2
page 7 U1-5; U3-4,6; U4-7,8; U5-1,5
page 8 R15-1; U7-9, 17, 29, 41
page 9 U8-1, 8; U9-1,3,8; U10-1,8; U11-5; U12-5; U13-1
page 10 L1-1
page 12 U18-2,5
page 13 U21-1
page 14 R54-1
page 15 R71-1
pag3 16 R86-1
page 17 U46-7,23,48,51,63; U47-4
        R106-R10 pin 1; R112-R115 pin 1
page 18  U48-8; R119-1; R120-1
         U49-8; R123-1; R124-1
         U50-8; R127-1; R128-1
-----------------------------------------
Net- n3V3  (-3.3Vdc) Supply 50mA
Source - page 11 U18-1; NCP1729SN35T1
Circuit
page 6 H1-29; TP29
page 9 U8-5; U9-5; U10-5
-----------------------------------------
Net- 1V8  1.8Vdc Supply 350mA
Source- page 11 U19-5
Circuit
page 6 H1-31; TP31
page 17 U46-17,49,63; R102-1
```

LAYOUT RULES

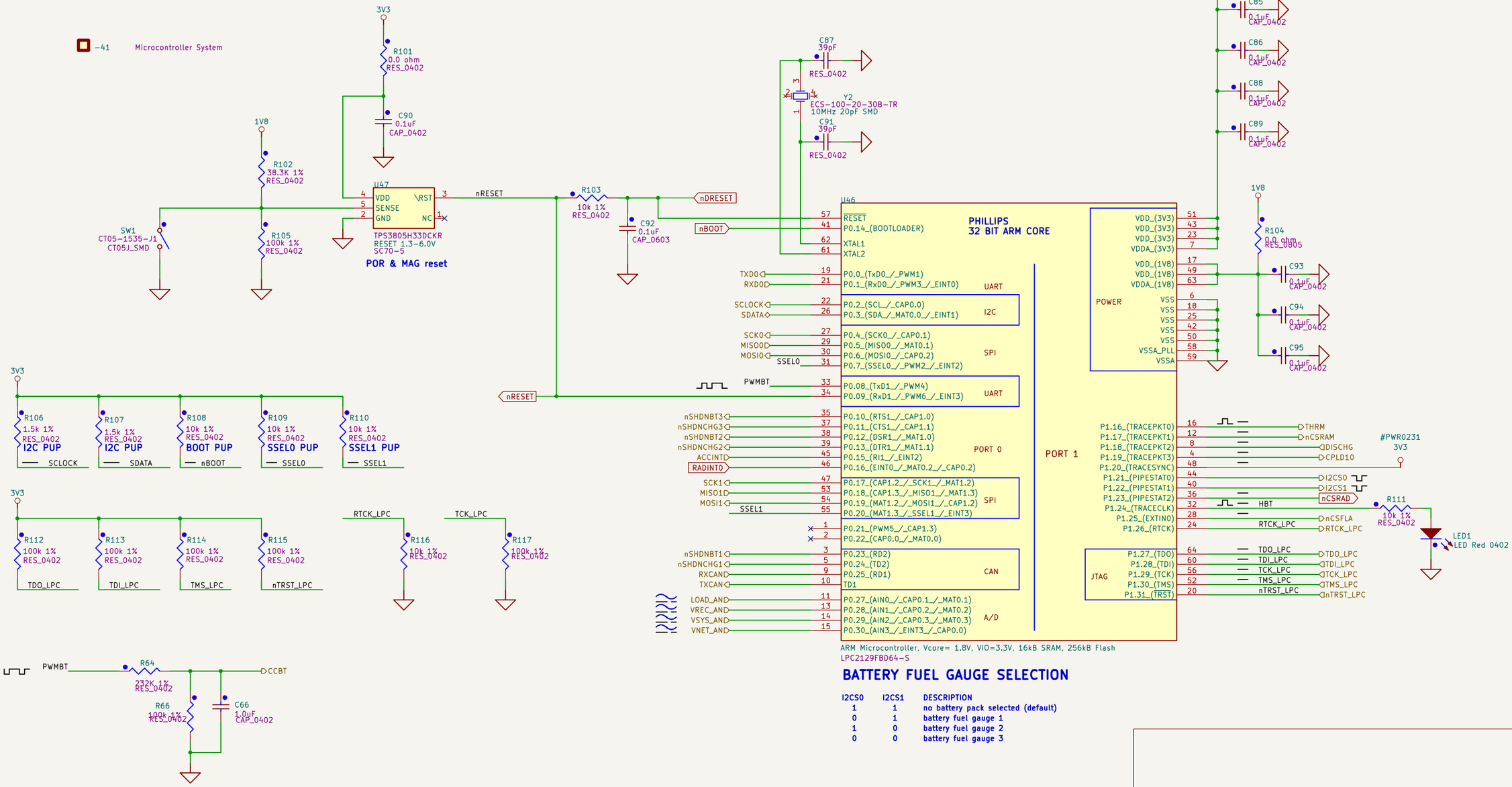
CUTOUT PLANES AND DO NOT ROUTE UNDERNEATH HIGH CURRENT SWITCHING LOOPS

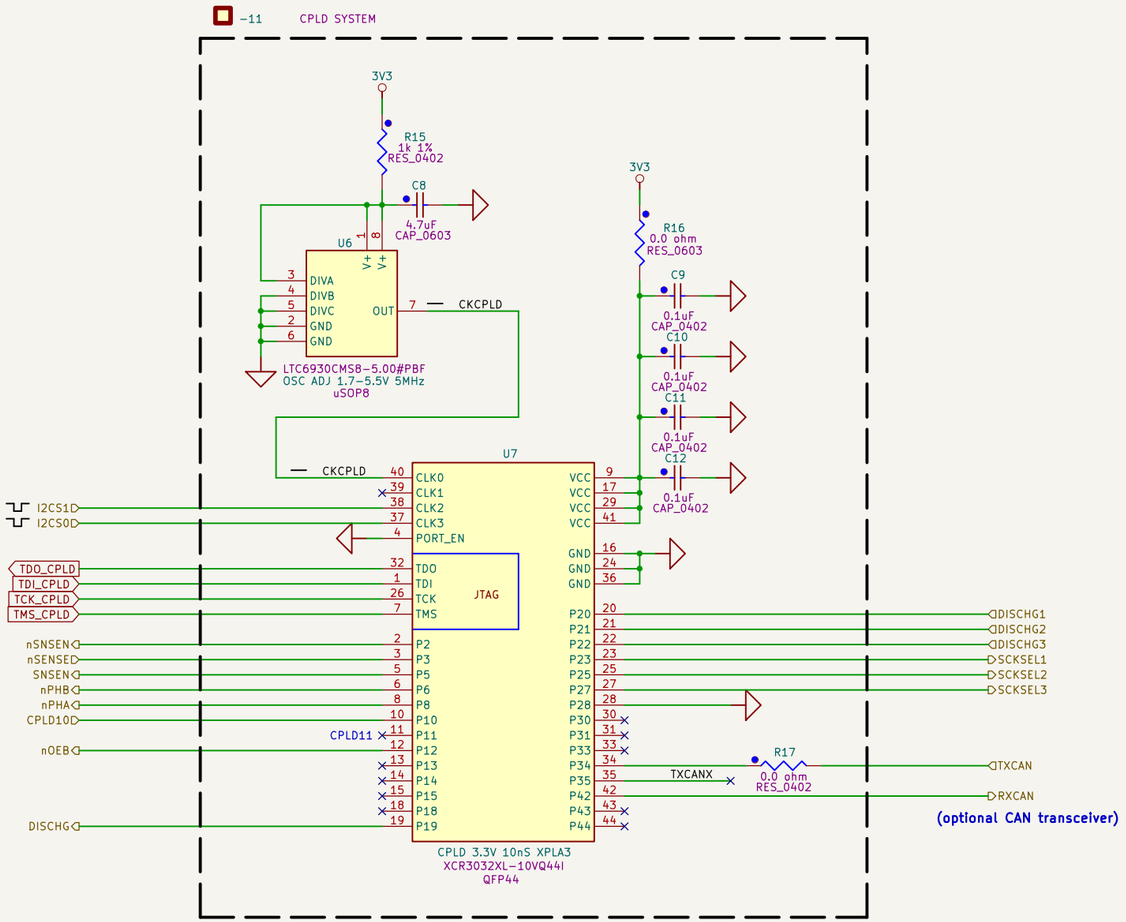
Sheet: /Power Supply/	
File: PM1C_Rev_1_Power_Supply.kicad_sch	
Title:	
Size: B	Date:
KiCad E.D.A. 8.0.2	**Rev: -**
	Id: 1/20

-27 NETWORK POWER SUPPLY SYSTEM



Sheet: /Network Power/		
File: PM1C_Rev_1_Network_Power.kicad_sch		
Title:		
Size: B	Date:	**Rev: –**
KiCad E.D.A. 8.0.2		Id: 1/20


-41 Microcontroller System
3V3
R101
0.0 ohm
RES_0402
C90
0.1uF
CAP_0402
1V8
R102
38.3K 1%
RES_0402
R105
100k 1%
RES_0402
SW1
CT05-1535-J1
CT05J_SMD
U47
VDD
SENSE
GND
\RST
NC
TPS3805H33DCKR
RESET 1.3-6.0V
SC70-5
POR & MAG reset
nRESET
R103
10k 1%
RES_0402
C92
0.1uF
CAP_0603
nDRESET
nBOOT
C87
39pF
RES_0402
Y2
ECS-100-20-30B-TR
10MHz 20pF SMD
C91
39pF
RES_0402
U46
RESET
P0.14_(BOOTLOADER)
XTAL1
XTAL2
PHILLIPS
32 BIT ARM CORE
TXD0
RXD0
P0.0_(TxD0_/_PWM1)
P0.1_(RxD0_/_PWM3_/_EINT0)
UART
SCLOCK
SDATA
P0.2_(SCL_/_CAP0.0)
P0.3_(SDA_/_MAT0.0_/_EINT1)
I2C
SCK0
MISO0
MOSI0
SSEL0
P0.4_(SCK0_/_CAP0.1)
P0.5_(MISO0_/_MAT0.1)
P0.6_(MOSI0_/_CAP0.2)
P0.7_(SSEL0_/_PWM2_/_EINT2)
SPI
PWMBT
P0.08_(TxD1_/_PWM4)
P0.09_(RxD1_/_PWM6_/_EINT3)
UART
nSHDNBT3
nSHDNCHG3
nSHDNBT2
nSHDNCHG2
ACCINT
RADINT0
P0.10_(RTS1_/_CAP1.0)
P0.11_(CTS1_/_CAP1.1)
P0.12_(DSR1_/_MAT1.0)
P0.13_(DTR1_/_MAT1.1)
P0.15_(RI1_/_EINT2)
P0.16_(EINT0_/_MAT0.2_/_CAP0.2)
PORT 0
SCK1
MISO1
MOSI1
SSEL1
P0.17_(CAP1.2_/_SCK1_/_MAT1.2)
P0.18_(CAP1.3_/_MISO1_/_MAT1.3)
P0.19_(MAT1.2_/_MOSI1_/_CAP1.2)
P0.20_(MAT1.3_/_SSEL1_/_EINT3)
SPI
P0.21_(PWM5_/_CAP1.3)
P0.22_(CAP0.0_/_MAT0.0)
nSHDNBT1
nSHDNCHG1
RXCAN
TXCAN
TD1
P0.23_(RD2)
P0.24_(TD2)
P0.25_(RD1)
CAN
LOAD_AN
VREC_AN
VSYS_AN
VNET_AN
P0.27_(AIN0_/_CAP0.1_/_MAT0.1)
P0.28_(AIN1_/_CAP0.2_/_MAT0.2)
P0.29_(AIN2_/_CAP0.3_/_MAT0.3)
P0.30_(AIN3_/_EINT3_/_CAP0.0)
A/D
PORT 1
POWER
VDD_(3V3)
VDD_(3V3)
VDD_(3V3)
VDDA_(3V3)
VDD_(1V8)
VDD_(1V8)
VDDA_(1V8)
VSS
VSS
VSS
VSS
VSS
VSSA_PLL
VSSA
P1.16_(TRACEPKT0)
P1.17_(TRACEPKT1)
P1.18_(TRACEPKT2)
P1.19_(TRACEPKT3)
P1.20_(TRACESYNC)
P1.21_(PIPESTAT0)
P1.22_(PIPESTAT1)
P1.23_(PIPESTAT2)
P1.24_(TRACECLK)
P1.25_(EXTIN0)
P1.26_(RTCK)
THRM
nCSRAM
DISCHG
CPLD10
I2CS0
I2CS1
nCSRAD
HBT
nCSFLA
RTCK_LPC
JTAG
P1.27_(TDO)
P1.28_(TDI)
P1.29_(TCK)
P1.30_(TMS)
P1.31_(TRST)
TDO_LPC
TDI_LPC
TCK_LPC
TMS_LPC
nTRST_LPC
ARM Microcontroller, Vcore= 1.8V, VIO=3.3V, 16kB SRAM, 256kB Flash
LPC2129FBD64-S
3V3
R100
0.0 ohm
RES_0805
C85
C86
C88
C89
0.1uF
CAP_0402
1V8
R104
0.0 ohm
RES_0805
C93
C94
C95
#PWR0231
3V3
R111
10k 1%
RES_0402
LED1
LED Red 0402
R106
1.5k 1%
RES_0402
I2C PUP
R107
1.5k 1%
RES_0402
I2C PUP
R108
10k 1%
RES_0402
BOOT PUP
R109
10k 1%
RES_0402
SSEL0 PUP
R110
10k 1%
RES_0402
SSEL1 PUP
R112
100k 1%
RES_0402
R113
100k 1%
RES_0402
R114
100k 1%
RES_0402
R115
100k 1%
RES_0402
R116
10k 1%
RES_0402
R117
100k 1%
RES_0402
R64
232K 1%
RES_0402
R66
100k 1%
RES_0402
C66
1.0uF
CAP_0402
CCBT
BATTERY FUEL GAUGE SELECTION
I2CS0 I2CS1 DESCRIPTION
1 1 no battery pack selected (default)
0 1 battery fuel gauge 1
1 0 battery fuel gauge 2
0 0 battery fuel gauge 3
Sheet: /Microcontroller/
File: PM1C_Rev_1_Microcontroller.kicad_sch
Title:
Size: B
Date:
Rev: -
KiCad E.D.A. 8.0.2
Id: 1/20



CPLD NOTES

1) Program U7 with PM20 code.

2) Power rail noise on oscillator causes output jitter. LPF Fc of 34 Hz determined empirically from PM1A. Fc = 1/(2*pi*R*C)

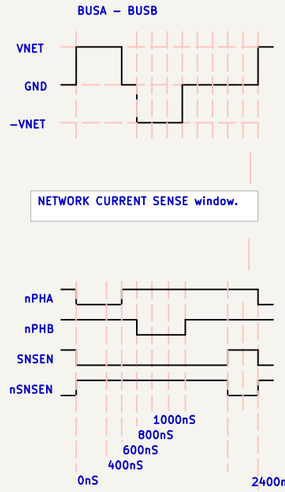
3) Either TXCAN (from CPU) or TXCANX (from optional CAN transceiver) should be used.

CAN BIT DECODING

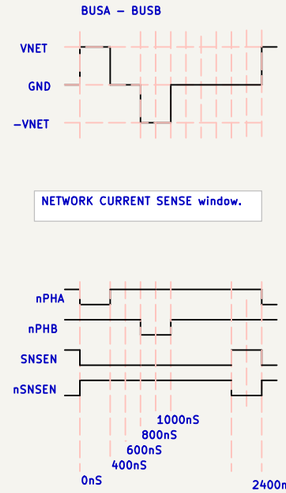
Logic 1 = RECESSIVE
Logic 0 = DOMINANT

FESCAN BIT DECODING

RECESSIVE



DOMINANT



NOTES:
1) Width of (BUSA - BUSB) voltage pulse determines remote module receive bit (0 or 1)
2) Current on bus at 2000ns indicates remote module transmit bit
3) Ref PRJ-NNPS-SYS-REP-04
4) Bold traces carry up to 500mA, 15nS edges

Sheet: /CPLD/		
File: PM1C_Rev_1_CPLD.kicad_sch		
Title:		
Size: B	Date:	**Rev: -**
KiCad E.D.A. 8.0.2		Id: 1/20

CURRENT SENSE NOTES

1) 20 ohm load during network current sense interval empirically determined to provide best compromise between signal amplitude and noise immunity when sensing 1mA talkbalk current amplitude

2) Resistor divider set to provide a 15mV reference level for comparator

-13 NETWORK CURRENT SENSE SYSTEM

VNET
R19
0.0 ohm
RES_0603
C15
0.1uF
CAP_0402
SENSE
U9
VS+
OE
IN
GND
VS-
VH
OUT
VL
EL7156CSZ
Pin driver 15nS
Narrow SO8
SNSEND
n3V3
BUSA
CURSENSE
R23
20 ohm 1%
RES_0805
3V3
R24
0.0 ohm
RES_0603
C20
0.1uF
CAP_0402
U13
IN
GND
OUT
SOT23-3
MAX6018AEUR21+T
REF 2.048V 5uA
NETREF
C21
1000pF
CAP_0402
R25
100k 1%
SM_0805
DIVNETREF
R26
750 ohm 1%
RES_0805
C22
1000pF
CAP_0402
3V3
R20
0.0 ohm
RES_0603
C16
0.1uF
CAP_0402
U11
VCC
GND
SC70-5
MAX9140EXK+T
CMP 2.7-5.5V 40ns
SENSE
3V3
R22
0.0 ohm
RES_0603
C18
0.1uF
CAP_0402
U12
VCC
IN
GND
OUT
NC
SC70-5
NC7SZ14P5X
UHS Inverter,
nSENSE

-12 NETWORK DRIVE SYSTEM

VNET
R18
0.0 ohm
RES_0603
PHASE A
C13
4.7uF
CAP_0805
U8
VS+
OE
IN
GND
VS-
VH
OUT
VL
EL7156CSZ
Pin driver 15nS
Narrow SO8
nSNSEND
nPHAD
n3V3
BUSA
C14
0.1uF
CAP_0402
BUSB
VNET
R21
0.0 ohm
RES_0603
PHASE B
C17
4.7uF
CAP_0805
U10
VS+
OE
IN
GND
VS-
VH
OUT
VL
EL7156CSZ
Pin driver 15nS
Narrow SO8
nOEB
nPHB
n3V3
C19
0.1uF
CAP_0402

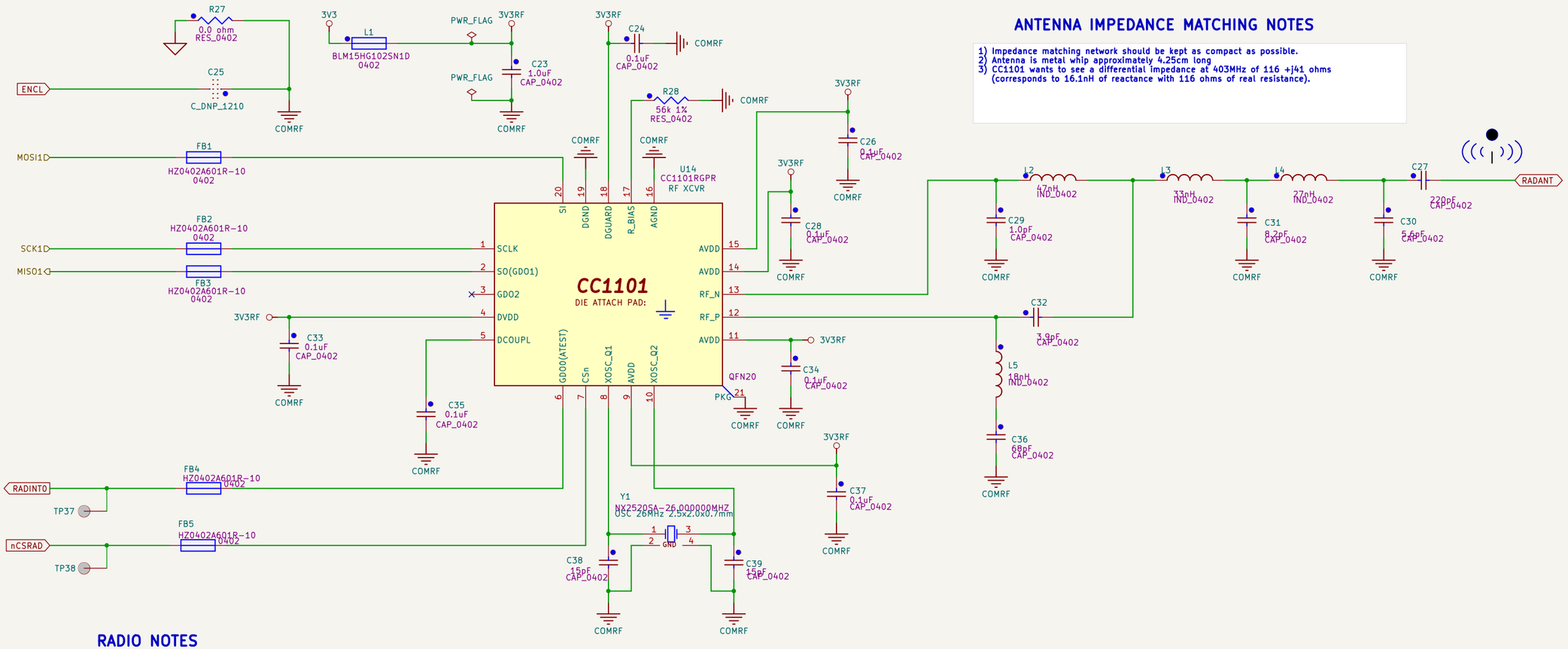
PIN DRIVER NOTES

OE	IN	OUT
0	x	High Z
1	0	VH
1	1	VL

Sheet: /Network Drive & Network Current Sense/
File: PM1C_Rev_1_Network_Drive.kicad_sch

Title:

Size: B | Date: | **Rev: –**
KiCad E.D.A. 8.0.2 | Id: 1/20



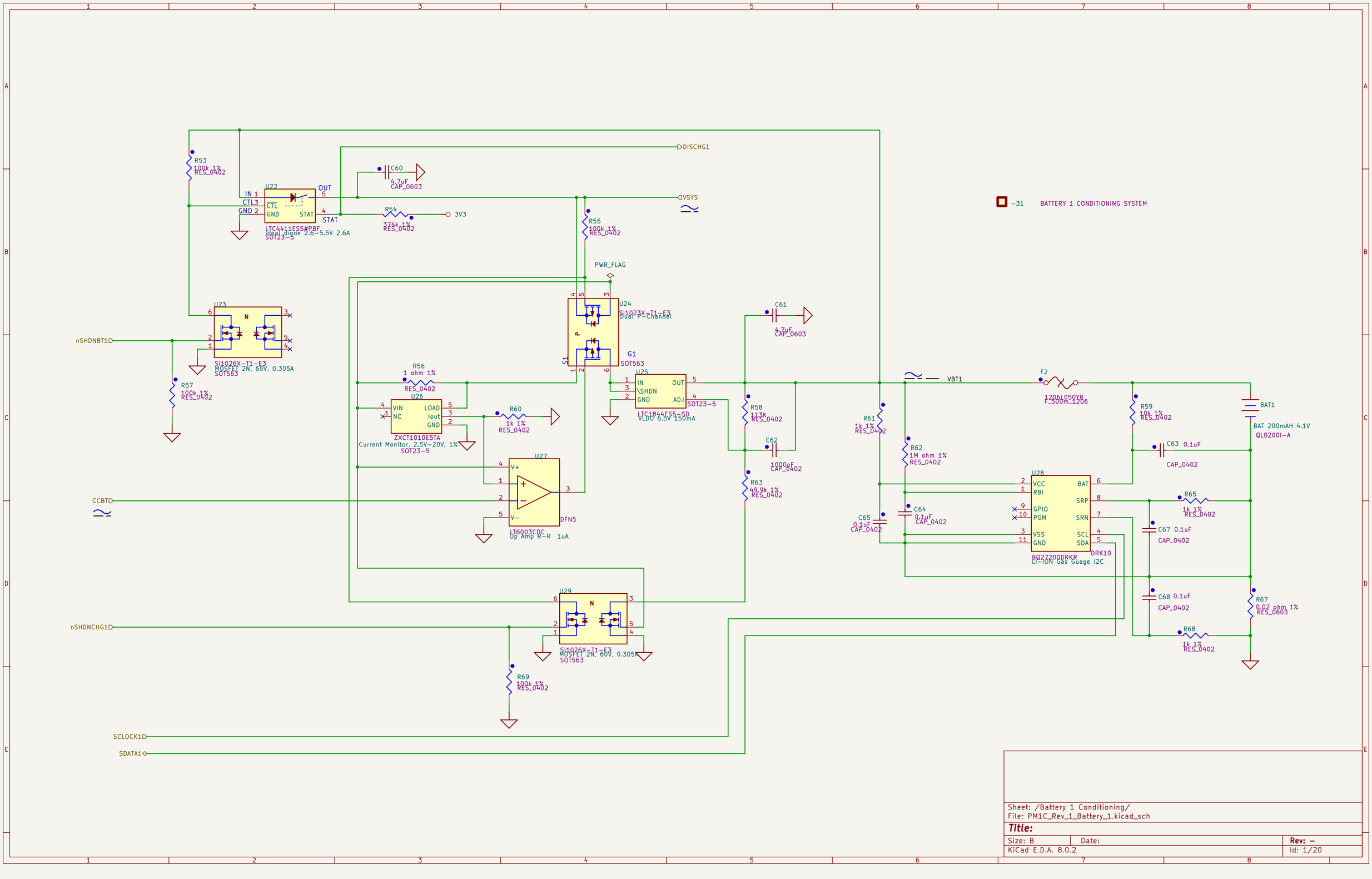
ANTENNA IMPEDANCE MATCHING NOTES

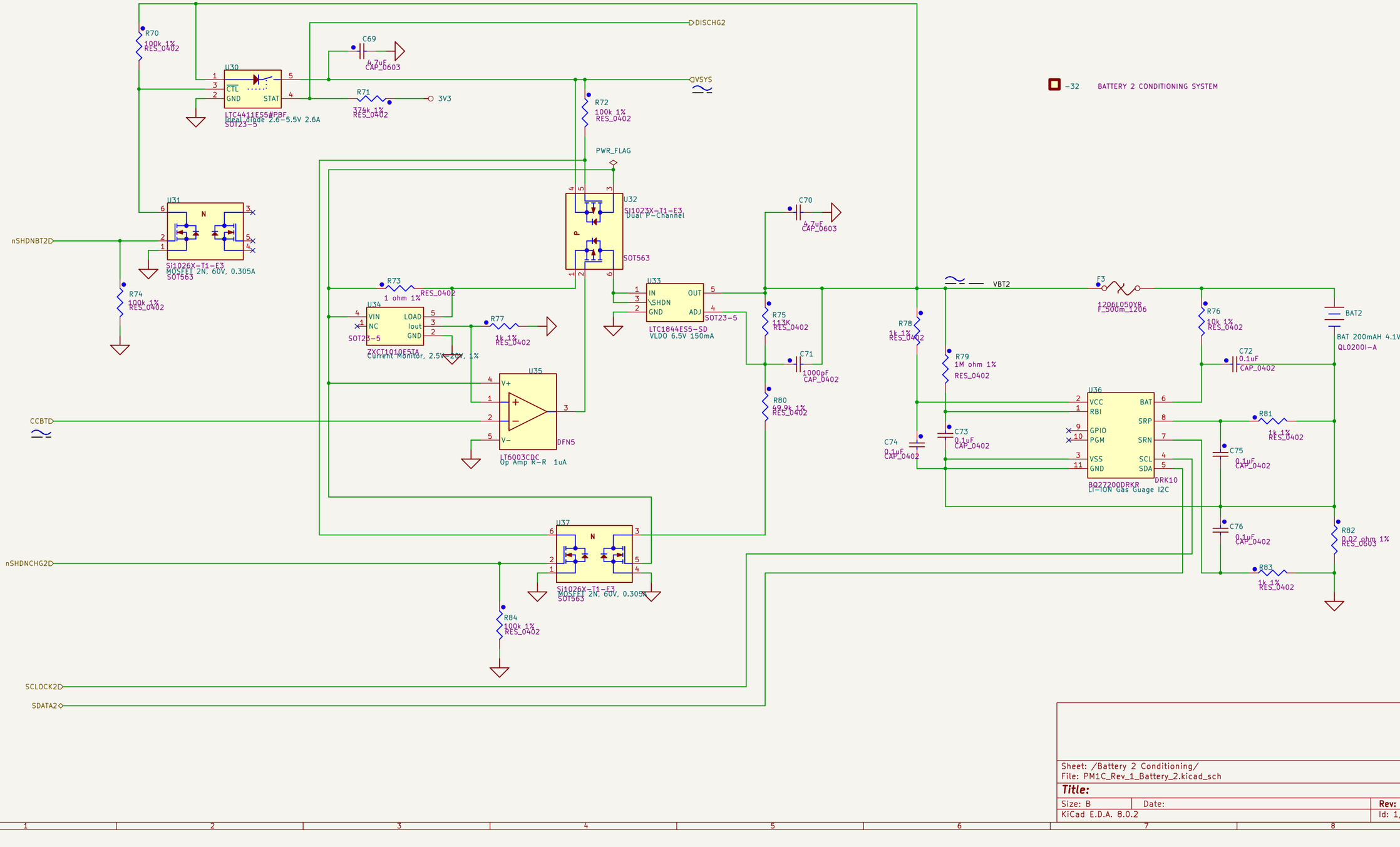
1) Impedance matching network should be kept as compact as possible.
2) Antenna is metal whip approximately 4.25cm long
3) CC1101 wants to see a differential impedance at 403MHz of 116 +j41 ohms
   (corresponds to 16.1nH of reactance with 116 ohms of real resistance).

RADIO NOTES

1) USE SOLID GROUND PLANE IN LAYOUT
2) Ref section 29 "PCB Layout Recommendations" in Texas Instruments CC1101 datasheet SWRS061C p. 54.
3) Series ferrites on digital lines intended to reduce RF noise coupling back to processor.

Sheet: /MED Radio/		
File: PM1C_Rev_1_MED_Radio.kicad_sch		
Title:		
Size: B	Date:	**Rev: –**
KiCad E.D.A. 8.0.2		Id: 1/20


-31 BATTERY 1 CONDITIONING SYSTEM
R53
100k 1%
RES_0402
U22
IN 1
CTL 3
GND 2
OUT
STAT
LTC4411ES5#PBF
Ideal diode 2.6-5.5V 2.6A
SOT23-5
C60
4.7uF
CAP_0603
R54
374k 1%
RES_0402
3V3
DISCHG1
VSYS
R55
100k 1%
RES_0402
PWR_FLAG
U23
nSHDNBT1
Si1026X-T1-E3
MOSFET 2N, 60V, 0.305A
SOT563
R57
100k 1%
RES_0402
U24
Si1023X-T1-E3
Dual P-Channel
G1
SOT563
C61
4.7uF
CAP_0603
R56
1 ohm 1%
RES_0402
U26
VIN
NC
LOAD
Iout
GND
ZXCT1010E5TA
Current Monitor, 2.5V-20V, 1%
SOT23-5
R60
1k 1%
RES_0402
U25
IN
SHDN
GND
OUT
ADJ
SOT23-5
LTC1844ES5-SD
VLDO 6.5V 150mA
R58
113K
RES_0402
C62
1000pF
CAP_0402
R63
49.9k 1%
RES_0402
VBT1
F2
1206L050YR
F_500m_1206
R61
1k 1%
RES_0402
R62
1M ohm 1%
RES_0402
U27
V+
V-
DFN5
LT6003CDC
Op Amp R-R 1uA
CCBTD
U28
VCC
RBI
GPIO
PGM
VSS
GND
BAT
SRP
SRN
SCL
SDA
DRK10
BQ27200DRKR
LI-ION Gas Guage I2C
C65
0.1uF
CAP_0402
C64
0.1uF
CAP_0402
BAT1
BAT 200mAH 4.1V
QL0200I-A
R59
10k 1%
RES_0402
C63 0.1uF
CAP_0402
R65
1k 1%
RES_0402
C67 0.1uF
CAP_0402
C68 0.1uF
CAP_0402
R67
0.02 ohm 1%
RES_0603
R68
1k 1%
RES_0402
U29
nSHDNCHG1
Si1026X-T1-E3
MOSFET 2N, 60V, 0.305A
SOT563
R69
100k 1%
RES_0402
SCLOCK1
SDATA1
Sheet: /Battery 1 Conditioning/
File: PM1C_Rev_1_Battery_1.kicad_sch
Title:
Size: B
Date:
Rev: -
KiCad E.D.A. 8.0.2
Id: 1/20



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File: PM1C_Rev_1_Battery_2.kicad_sch

Title:

Size: B	Date:	**Rev: –**
KiCad E.D.A. 8.0.2		Id: 1/20

-33 BATTERY 3 CONDITIONING SYSTEM

R85
100k 1%
RES_0402

U38
LTC4411ES5#PBF
Ideal diode 2.6-5.5V 2.6A
SOT23-5

C77
4.7uF
CAP_0603

R86
374k 1%
RES_0402

DISCHG3
VSYS
3V3

R87
100k 1%
RES_0402

PWR_FLAG

U39
Si1026X-T1-E3
MOSFET 2N, 60V, 0.305A
SOT563

nSHDNBT3

R89
100k 1%
RES_0402

U40
SI1023X-T1-E3
Dual P-Channel
SOT563

C78
4.7uF
CAP_0603

R88 1 ohm 1%
RES_0402

U41
LTC1844ES5-SD
VLDO 6.5V 150mA
SOT23-5

U42
ZXCT1010E5TA
Current Monitor, 2.5V-20V, 1%
SOT23-5

R92
1k 1%
RES_0402

R90
113K
RES_0402

C79
1000pF
CAP_0402

R95
49.9k 1%
RES_0402

U43
Op Amp R-R 1uA
LT6003CDC
DFN5

CCBTD

VBT3

F4
1206L050YR
F_500m_1206

R93
1k 1%
RES_0402

R94
1M ohm 1%
RES_0402

R91
10k 1%
RES_0402

BAT3
BAT 200mAH 4.1V
QL0200I-A

C80
0.1uF
CAP_0402

U44
BQ27200DRKR
LI-ION Gas Guage I2C
DRK10

C81
0.1uF
CAP_0402

C82
0.1uF
CAP_0402

R96
1k 1%
RES_0402

C83
0.1uF
CAP_0402

C84
0.1uF
CAP_0402

R97
0.02 ohm 1%
RES_0603

R98
1k 1%
RES_0402

U45
Si1026X-T1-E3
MOSFET 2N, 60V, 0.305A
SOT563

nSHDNCHG3

R99
100k 1%
RES_0402

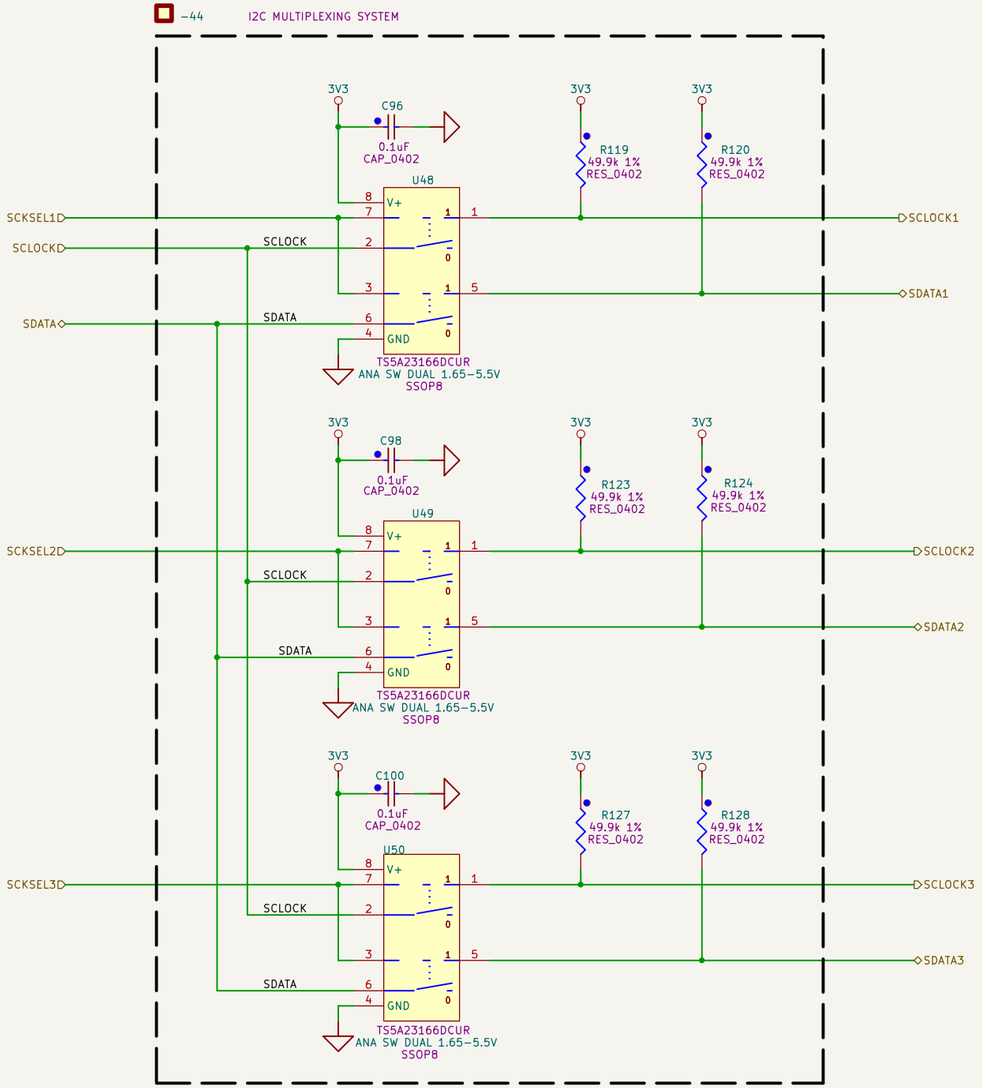
SCLOCK3

SDATA3

Sheet: /Battery 3 Conditioning/
File: PM1C_Rev_1_Battery_3.kicad_sch

Title:

Size: B	Date:	Rev: –
KiCad E.D.A. 8.0.2		Id: 1/20

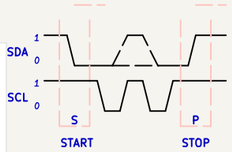


I2C INTERFACING NOTES

* Pull up I2C line when main I2C pullup not connected.
* Disconnect both clock and data lines when removing a device from the I2C bus.

RATIONALE:
Both clock and data lines must be pulled up to indicate an inactive bus (per attached figure).

SOURCE: PHILIPS SEMICONDUCTOR,THE I2C-BUS SPECIFICATION VERSION 2.1, JANUARY 2000



Sheet: /I2C Multiplexing/
File: PM1C_Rev_1_I2C_Multiplexing.kicad_sch

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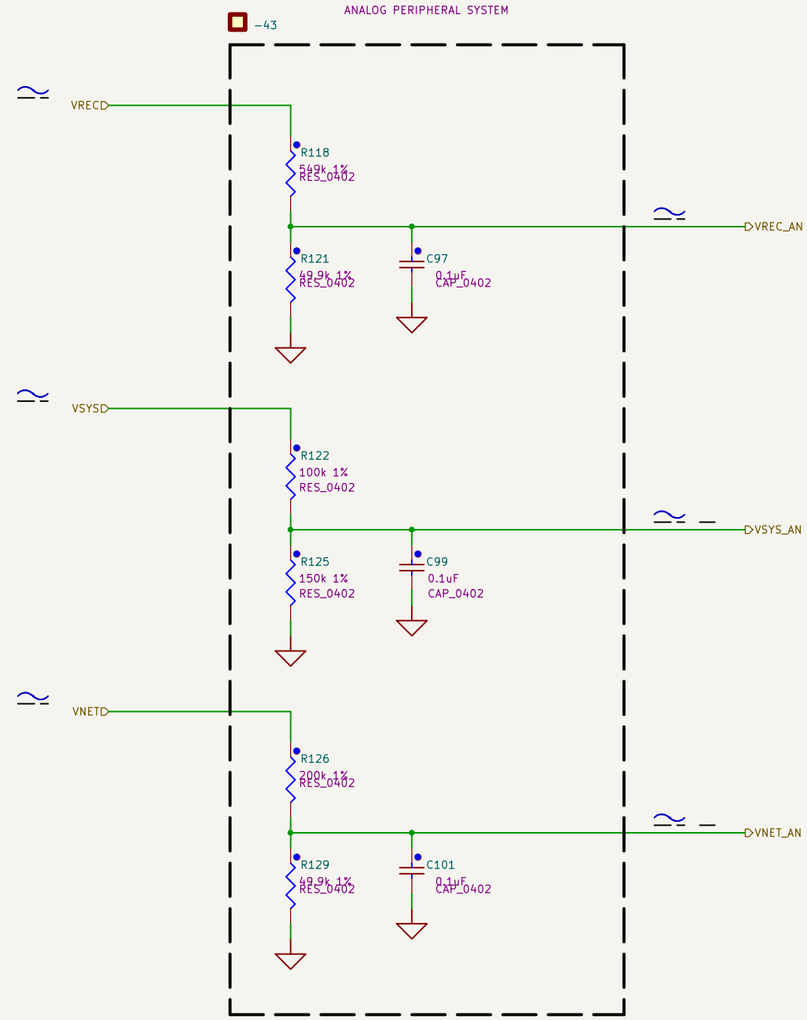
Size: B	Date:	**Rev: -**
KiCad E.D.A. 8.0.2		Id: 1/20



Sheet: /Analog Voltage Monitoring/
File: PM1C_Rev_1_Analog_Monitoring.kicad_sch

Title:

Size: B	Date:	**Rev: –**
KiCad E.D.A. 8.0.2		Id: 1/20

VOLTAGE REFERENCE NOTES

Voltage reference output capacitance needs to be at least 100pF for stability but small enough to allow pulse powering from a microprocessor digital output pin.

The 5µA maximum supply current varies only 0.1µA/V with the supply voltage. When the supply voltage is below the minimum-specified input voltage (as during turn-on), the devices can draw up to 20µA beyond the nominal supply current. The input voltage source must be capable of providing this current to ensure reliable turn-on.

-2 ENCLOSURE THERMISTOR SYSTEM

THRM

U2
MAX6018AEUR21-T
REF 2.048V 5uA
SOT23-3

C4
0.1uF
CAP_0402

R10
7.5k 1%
RES_0402

C2
1000pF
CAP_0402

RV1
MA100BF103A
Thru-Hole

C5
1000pF
CAP_0402

3V3

C1
0.1uF
CAP_0402

I2C ADC
U1
ADS1110A0IDBVT
I2C address 1001000
SOT23-6

SCLOCK

SDATA

-42 DIGITAL PERIPHERAL SYSTEM

3V3MEM

R9
30k 1%
RES_0402

nWPMEM

R12
R_DNP_0402

3V3

R11
0.0 ohm
RES_0603

C3
0.1uF
CAP_0402

nCSFLA

SCK0

MOSI0

U3
AT45DB321E-SHF-T
Flash 2.7-3.6V 32Mbit SPI
SOIC, 8-Leads

MISO0

R13
0.0 ohm
RES_0603

C6
0.1uF
CAP_0402

nCSRAM

U4
23K256T-I/ST-ND
RAM, 256Kbit, SPI
8-Lead [TSSOP]

U5
ISM330ISTR
6-axis IMU
I2C Address: 1101010b (Write D4h, Read D5h)

SCLOCK

SDATA

3V3

R14
3.0k
RES_0402

C7
0.1uF
CAP_0402

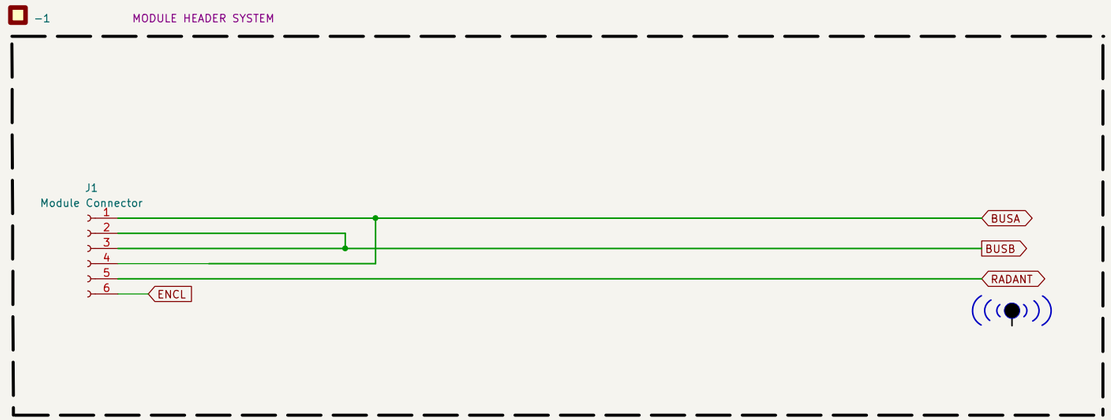
NNPS:LGA-14L_STM

ACCINT

Sheet: /Thermister & Digital Peripheral System/
File: PM1C_Rev_1_Thermister_and_Accelerometer.kicad_sch

Title:

Size: B | Date: | **Rev: -**
KiCad E.D.A. 8.0.2 | Id: 1/20



Sheet: /Module Connector/
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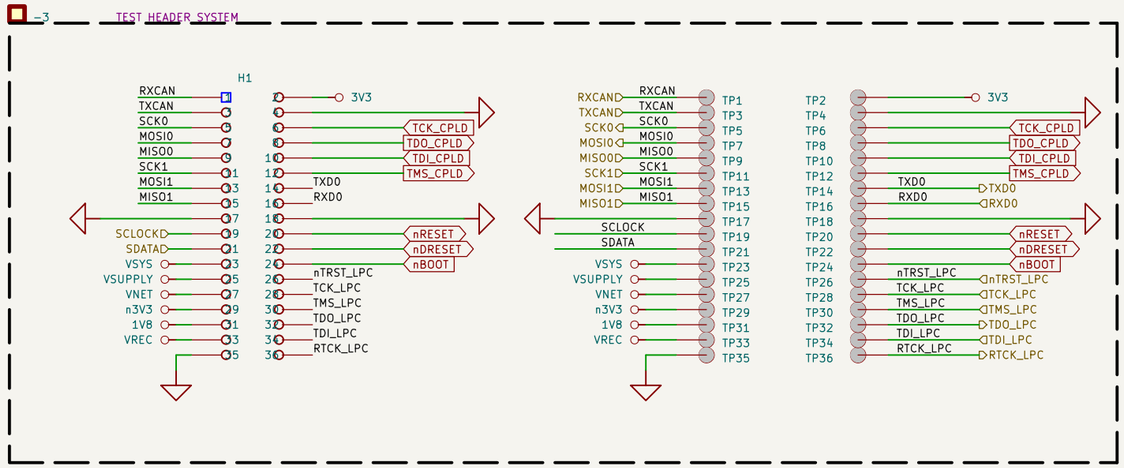
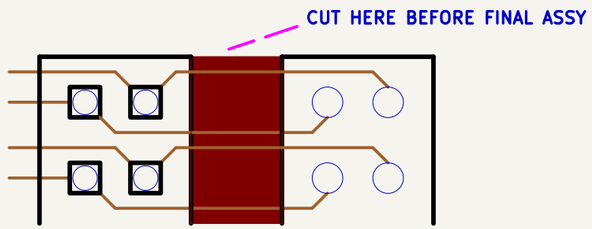
KiCad E.D.A. 8.0.2		Id: 1/20



LR2: Stagger traces on different layers running to the cut-away header Do not place adjacent-layer copper traces



Sheet: /Test Points/
File: PM1C_Rev_1_Test_Connector.kicad_sch

Title:

Size: B | Date: | **Rev: –**

KiCad E.D.A. 8.0.2 | Id: 1/20